

# A Novel Design of Power-Efficient and Accurate Approximate Multiplier using Approximate Compressors and Approximate Adders

Mrs. C. Munikantha<sup>1</sup>, C. Prathyusha<sup>2</sup>, B. Sudarshan<sup>3</sup>, N. Sasidhar Raju<sup>4</sup>, M. Purushotham<sup>5</sup>

<sup>1</sup> Assistant Professor, Department of Electronics & Communication Engineering , Annamacharya Institute Of Technology & Sciences, Tirupati, Andhra Pradesh, India, [chinthaguntamuni9@gmail.com](mailto:chinthaguntamuni9@gmail.com)

<sup>2</sup> U.G Scholar, Department of Electronics & Communication Engineering , Annamacharya Institute Of Technology & Sciences, Tirupati, Andhra Pradesh, India, [prathyushac75@gmail.com](mailto:prathyushac75@gmail.com)

<sup>3</sup> U.G Scholar, Department of Electronics & Communication Engineering , Annamacharya Institute Of Technology & Sciences, Tirupati, Andhra Pradesh, India, [birusudarshan777@gmail.com](mailto:birusudarshan777@gmail.com)

<sup>4</sup> U.G Scholar, Department of Electronics & Communication Engineering , Annamacharya Institute Of Technology & Sciences, Tirupati, Andhra Pradesh, India, [sasidharraju867@gmail.com](mailto:sasidharraju867@gmail.com)

<sup>5</sup> U.G Scholar, Department of Electronics & Communication Engineering , Annamacharya Institute Of Technology & Sciences, Tirupati, Andhra Pradesh, India, [purushothampurna123@gmail.com](mailto:purushothampurna123@gmail.com)

\*\*\*

**Abstract** – This paper proposes a novel design of a power- efficient and accurate approximate multiplier that utilizes the concepts of approximate compressors and adders. In many applications, such as image processing, neural networks, and wireless communications, the requirement of precision may not be high. Therefore, the use of approximate computing techniques may be used to improve the performance and reduce the power consumption. In this paper, the design of the multiplier is simplified with the use of approximate logic blocks, which include the use of approximate half adders, full adders, and compressors. In addition, the design includes an error compensation mechanism that ensures the design is accurate. In this paper, the design is coded using Verilog HDL and then simulated and synthesized using the Xilinx Vivado tool. The simulation results reveal that the designs proposed in this paper significantly reduce the power consumption while ensuring the accuracy of the designs. In this paper, the proposed design is compared with the existing designs, where the power consumption is reduced by 59.16% and 65.93%, with average accuracies of 93.14% and 91.98%, respectively.

**Keywords:** Reduced power, Increased speed, Decrease area, Accuracy is increased.

## 1. INTRODUCTION

Multiplication is a very important arithmetic operation used in many digital systems and computing applications. This operation is used in many applications such as digital signal processing, image processing, machine learning, artificial intelligence, communication systems, etc. The arithmetic circuits used in traditional computing systems are designed to give completely accurate results. However, to obtain accurate results in computing systems, complex hardware circuits are used. This results in an increase in power consumption and processing time.

However, in recent electronic devices, especially in portable electronic devices that are battery- powered, minimizing power consumption and maximizing processing speed are very important issues. To resolve these issues in computing systems, a new concept known as approximate computing has been introduced. The concept of approximate computing is to introduce a certain level of errors in computing systems in order to obtain a significant reduction in hardware complexity, power consumption, and processing

time. Many applications in real-life computing systems, such as multimedia processing and image processing, can tolerate a certain level of errors because these errors are not recognizable by humans. Out of various approximate circuits, the approximate multipliers have drawn much more interest, as multiplication operations are often performed for various computational operations. An approximate multiplier performs multiplication operations with reduced hardware complexity, considering minor errors in the output. Compared to the exact multipliers, the approximate multipliers consume less power, occupy less chip area, and operate faster.

These advantages of the approximate multipliers enable the use of these multipliers for various applications where errors are allowed. The approximate multipliers are designed by modifying the internal components of the multipliers, i.e., compressors and adders, to reduce the complexity of the multipliers.

Compressors are often used in the multiplier architectures to reduce the multiple partial products to fewer bits, thereby speeding up the multiplication process. Approximate compressors simplify the multiplication process by considering minor errors, ignoring the rare combinations of inputs, or performing logic operations. Similarly, the use of approximate adders is utilized to reduce the complexity of the design. In this case, the complexity of the design is reduced by replacing the complex logic gates with simpler logic gates. For example, the use of the OR gate is used instead of the XOR gate used in the design of the sum output of the half adder. In this case, the OR gate uses fewer transistors compared to the XOR gate, which reduces the power consumption. In the design of the full adder, the use of the OR gate is similar to the use of the OR gate in the design of the half adder.

In this paper, a novel design of power-efficient and accurate approximate multiplication is proposed. In this design, the use of approximate compressors and adders is used. In this design, the hardware complexity and power consumption are reduced while the level of accuracy is high. In the proposed design, the architecture of the multiplier is designed with the use of exact and approximate techniques

along with the use of the error correction mechanism to reduce the inaccuracies that occur due to the use of the approximation techniques. In this design, the Verilog HDL is used to implement the design. The simulation and synthesis tools were used to verify the design. In the proposed design, the power consumption is reduced while the level of accuracy is high. Thus, this design is useful for the design of energy-efficient computing applications.

## 2. Literature Survey:

In recent years, approximate computing has attracted considerable attention for digital system design due to its ability to reduce power consumption, hardware complexity, and delay with acceptable accuracy. Among all the arithmetic in various applications such as image processing, neural network design, signal processing, and multimedia system design. Traditional multipliers are optimized for producing accurate results. However, these multipliers are power hungry. In recent years, many applications are not highly sensitive to computational accuracy. Therefore, researchers proposed an approximate multiplier to reduce accuracy with a large improvement in power efficiency.

Several studies have been conducted to design energy-efficient approximate multipliers using various architectural styles. One significant work has been carried out by researchers to propose an ultra-efficient approximate multiplier with a truncated region, an error compensation module, and an exact computation unit. In this work, the least significant bits of the product are truncated to reduce hardware complexity and power consumption. To improve the accuracy of this approximate multiplier, an error compensation module has been used to compensate for the errors introduced due to truncation. This work has successfully demonstrated the trade-off between computational accuracy and hardware efficiency.

Another area of research includes the use of compressor circuits in multiplier architectures. The compressor circuits are critical blocks that reduce partial products produced during multiplication. Several researchers have proposed an approximate 4-2 compressor design that reduces circuit complexity by considering a low probability of input combinations. The use of an approximate

compressor reduces the propagation delay, power, and area of the circuit with a marginal amount of error. The researchers have proved that the use of an approximate compressor improves the performance of the circuit for error-tolerant applications such as image processing and machine learning.

image processing, neural networks, and multimedia, it has been observed that a certain operations, multiplication is one of the most common operations used. Apart from compressors, approximate adders have also been explored in the context of low-power arithmetic circuits. The approximate half adders and full adders reduce the hardware implementation complexities of the circuits by using simple logic gates instead of complex ones. For example, the XOR gate in the calculation of the sum output of the adder is replaced with an OR gate in the approximate adder, which reduces the power consumption of the circuit as the OR gate requires fewer transistors compared to the XOR gate. The efficiency of the approximate adder in the reduction of energy consumption has been shown by researchers.

More research has also been done in the design of efficient multipliers by incorporating approximate compressors and adders in the design of popular multiplier architectures such as the Dadda multiplier. These designs have achieved an efficient balance between accuracy and power efficiency by using a combination of precise and imprecise components. Researchers have also proposed the use of majority-based imprecise compressors and recursive multipliers for better design efficiency. Energy-efficient designs of Dadda multipliers using voltage over-scaling have also been proposed for longer circuit life.

Recent studies have further improved approximate multiplier designs with the development of high-accuracy compressors to optimize the designs for applications that require error resilience. The designs are targeted to achieve power saving, reduced delays, and acceptable levels of accuracy. From the literature, it can be concluded that approximate multipliers using compressors and adders are promising techniques for developing power-efficient computing systems. The techniques

can be used to implement high-performance hardware designs that are suitable for applications where errors are tolerated, but power consumption and speed are critical factors.

### 3. EXISTING SYSTEM

The current model for approximate multipliers has emphasized hardware efficiency with a certain amount of error in the result obtained from the multiplication process.

In a amount of error in the result obtained from the multiplication process does not affect the output to a large extent.

Therefore, a new model known as an approximate multiplier has been proposed. The complexity involved in the arithmetic process for these multipliers results in a reduced power consumption, delay, and hardware area.

In the existing designs, the implementation of the approximate multipliers is generally carried out with the help of techniques such as partial product truncation, the use of approximate compressors, and the use of approximate adders. In the partial product truncation method, the least significant bits of the multiplication products are eliminated to simplify the design. Compressors play a significant role in the design of the multiplication process, where the partial products are reduced to a minimum. In the case of exact multiplication, the compressors used produce accurate results. However, the use of the compressor reduces the complexity of the design and the use of the adder to produce near-accurate results with minimal errors. In the case of the adder, the complex design is simplified with the use of the OR operation instead of the XOR operation, which reduces the power consumption.

Many of the available multiplier designs also include error compensation mechanisms that handle errors due to approximate components. These mechanisms adjust certain values or add values to the components to ensure that the accuracy level is within the desired range. Using the components of truncation, approximate compressors, approximate adders, and error correction, the available multiplier designs achieve an effective trade-off between power efficiency and accuracy. The proposed

approximate multipliers are highly effective in improving performance and power efficiency conventional digital system, the multipliers are usually designed to give an exact result.

However, this results in a large number of logic gates, power consumption, and an increased delay. However, with the current trends in various digital systems such as over traditional multipliers and are thus applicable in error-tolerant applications such as digital signal processing, artificial intelligence, and image processing.

**4. Proposed Model:** The proposed model is the current work is based on designing an efficient and precise approximate multiplier using approximate compressors and adders. The multiplication operation is one of the basic arithmetic operations that are used in digital systems such as image processing, neural networks, and signal processing. The conventional multipliers are designed to obtain precise results, but they are associated with increased hardware complexity, power consumption, and delays. However, in real-world scenarios, the error rate is tolerable, as it does not impact the final outcome of the system. The proposed model is based on the concept of applying approximate computing techniques to achieve reduced hardware complexity and power consumption without compromising the precision of the system.

consumption of the circuit, 50% of the generated partial products are replaced by an 8-bit constant value, "00000110." The truncation of the partial products is an effective way to minimize the number of logic operations in the proposed multiplier. The rest of the partial products are then processed using compressors and adders. The 4-2 compressors are employed in the initial stage of the multiplication operation to achieve some level of accuracy, followed by the use of approximate compressors in later stages to minimize power consumption and maximize speed. The compressors are effective in reducing the number of input bits to be combined and thus accelerate the multiplication operation.



Fig1: Behavioral Simulation

The proposed multiplier's architecture is based on an 8x8 multiplication operation and involves several stages that include the use of both exact and approximate components. In the initial stage, partial products are generated based on the input values. In order to minimize the complexity and power

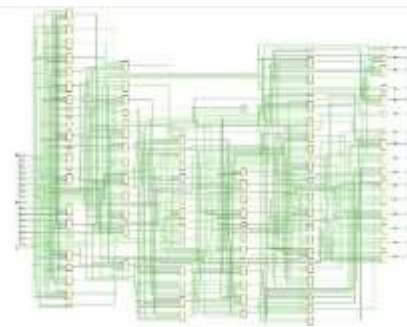


Fig2: Schematic Diagram

The design includes approximate adders such as half adders and full adders. These adders are included to further simplify the hardware implementation. In an approximate half adder, the XOR gate used for the sum calculation is replaced with an OR gate. This reduces the number of transistors used, thus reducing power consumption. In an approximate full adder, the sum calculation is modified, while the carry calculation remains the same. These design modifications simplify the gates and thus enhance the speed of the process. However, this design includes a controlled error. Since the design will be used for error-tolerant applications, this minor error will not be a problem.



Fig3: Circuit Diagram

Another significant part of the proposed model is the error correction mechanism. Due to the presence of inaccuracies in the design of the approximate compressor and partial products, the error compensation block is added to the design to ensure that the accuracy level is at a reasonable level. A correction value is generated as part of this block, which is used during the critical computation part. In the design, two OR gates are used to obtain the carry value used in the accurate part of the multiplication. The correction mechanism reduces the overall error that is accumulated due to the approximations. Thus, the design ensures that the multiplication is carried out with a reasonable balance between power efficiency and accuracy.

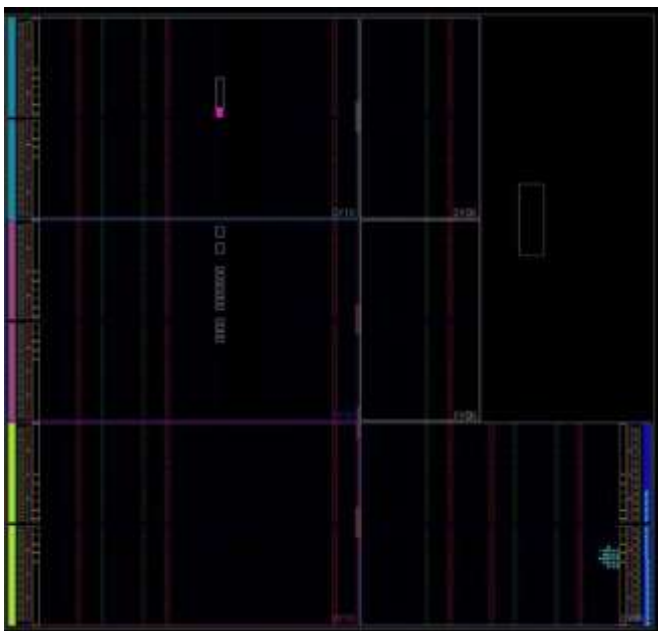


Fig4: IC physical design view

The architecture of the proposed model is such that there are two designs in the proposed architecture. The first is Design 1, in which the first stage of the proposed architecture consists of exact compressors, the second stage consists of approximate compressors, and the last stage consists of approximate adders in order to reduce the logic gates. The second is Design 2, in which the first and second stages of the proposed architecture consist of exact compressors, and the last stage consists of approximate full adders in order to reduce the power consumption of the proposed architecture. The results of the proposed architecture show that the power consumption of the proposed architecture is significantly reduced

compared to the conventional architecture of the multiplier. The proposed architecture is thus effective in the creation of an energy-efficient, high-speed multiplier.

## 5. References:

1. U. A. Kumar, P. Bikki, S. Veeramachaneni and S. E. Ahmed, "Power Efficient Approximate Multiplier Architectures for Error Resilient Applications," 2022 IEEE 19th India Council International Conference (INDICON), Kochi, India, 2022.
2. S. Rai, D. Guntuku, S. Gupta, M. M. D. Savio and M. Verma, "Design of low power approximate multiplier based on compressors for multimedia application," 2023 International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Communication, and Computational Intelligence (RAEEUCCI), Chennai, India, 2023.
3. D. B. S. S. G. Akhil, D. M. Reddy, G. Pardhasaradhi and P. S. Kumar, "Design and Analysis of Approximate Multipliers using Approximate 4:2 Compressors," 2023 IEEE 20th India Council International Conference (INDICON), Hyderabad, India, 2023.
4. Y. Zhang, X. Chen, P. Guo and G. Xie, "Design and Analysis of Approximate Multiplier of Majority-Based Imprecise 4-2 Compressor for Image Processing," 2023 IEEE 23rd International Conference on Nanotechnology (NANO), Jeju City, Korea, Republic of, 2023.
5. H. Waris, C. Wang, C. Xu, and W. Liu, "AxRMs: Approximate recursive multipliers using high-performance building blocks," *IEEE Trans. Emerg. Topics Comput.*, vol. 10, no. 2, pp1229–1235, Apr.–Jun. 2022.
6. H. Afzali-Kusha, M. Vaeztourshizi, M. Kamal and M. Pedram, "Design Exploration of Energy-Efficient Accuracy-Configurable Dadda Multipliers With Improved Lifetime Based on Voltage Overscaling," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*.