International Scientific Journal of Engineering and Management ISSN: 2583-6129
Volume: 03 Issue: 04 | April – 2024 DOI: 10.55041/ISJEM01526
An International Scholarly || Multidisciplinary || Open Access || Indexing in all major Database & Metadata

# Design and FPGA Implementation of 4x4 Vedic Multiplier using Different Architectures

**V. shyam sundhar[1], K.akhil2, N.suresh[3], T.sravan kumar [4], Mr. S. Rambabu[5]**

[1234]IV B. Tech, ECE Department, Santhiram Engineering College.

[5]Assistant Professor, ECE Department, Santhiram Engineering College.

---

**Abstract -** The need of high speed multiplier is increasing as the need of high speed processors are increasing. A Multiplier is one of the key hardware blocks in most of the fast processing systems which is not only a high delay block but also a major source of power dissipation. A conventional processor requires substantially more hardware resources and processing time in the multiplication operation, rather than addition and subtraction. This Project describes about the design of 4-bit, 8-bit and 32-bit Vedic multiplier using ancient Vedic mathematics which helps in delay and power reduction. Simulation is done in Xilinx VIVADO software using VHDL and display on LCD. The results for Vedic multiplier using various architecture and their delay comparison are done.

***Key Words*:** FPGA (Artix-7), adders, 4x4 Array Multiplier, Vedic Mathematics.

## 1. INTRODUCTION

A device with a matrix of reconfigurable gate array logic circuits is called an FPGA. An FPGA's internal circuitry is connected in such a way that it produces a hardware implementation of the software program when it is setup. FPGAs do not have an operating system and instead process logic using specialized hardware, unlike processors. Because FPGAs are really parallel devices, several processing processes do not have to compete with one another for the same resources. Uncommitted wires are used to route signals and a variety of logic modules form the foundation of FPGAs. The mask design used in the production of gate arrays connects these wires. As opposed to FPGAs, where the user connects these wires, these wires in FPGAs must be connected via an electronic device. The three most popular ways to accomplish this are through direct connects using Antifuse, flash or EEPROM carry the signal, or pass transistors operated by SRAM cells. The benefits and drawbacks of every one of these connectable devices vary. The design, architecture, and performance of the FPGA are significantly impacted by this.

*Vedic Multiplier:*

The Vedic multiplier formula (sutras) is the foundation of the suggested Vedic multiplier. The decimal numeral system has historically multiplied numbers using these sutras. To make the suggested method work with digital hardware, apply the same concepts to the binary numbers system. The following section discusses Vedic multiplication using an algorithm.

*Urdhva Triyagbhyam Sutra:*

In classical Indian mathematics, the Urdhva Triyagbhyam (vertical & crosswise) technique is the source of the multiplier. Urdhva Triyagbhyam Sutra Exists a general multiplication formula that applies to every possible scenario? The literal

International Scientific Journal of Engineering and Management
Volume: 03 Issue: 04 | April – 2024
An International Scholarly || Multidisciplinary || Open Access || Indexing in all major Database & Metadata
ISSN: 2583-6129
DOI: 10.55041/ISJEM01526

translation is "vertically and crosswise". This novel approach enables all partial goods to be generated and partial products to be inserted simultaneously.

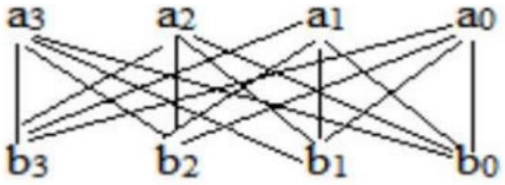



Fig (1) Existed Vedic Multiplier

*Vedic Multiplier For 2x2 Bit:*

The following is the procedure for two,2 bit numbers A and B, where, as indicated in the illustration, A=a1a0 and B=b1b0. First, the final product's least significant bit (LSB) (vertical).Next, the next higher bit of the multiplier is multiplied by the LSB of the multiplicand, and the product of the LSB of the multiplier and the next higher bit of the multiplicand is added (crosswise). The partial product formed by multiplying the most significant bits yields the sum and carry, which are added to the second bit of the final product. The third corresponding bit in the final result is the sum, while the fourth bit is carry. Vedic multiplier module is implemented using four input AND gates & two half-adder which is displayed in its block diagram in below figure The same method can be extended for higher no.of input bits. This section illustrates the implementation of 4x4 Vedic multiplier which uses 2x2 bit Vedic multiplier as a basic module.

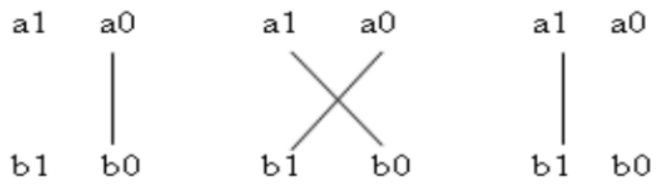
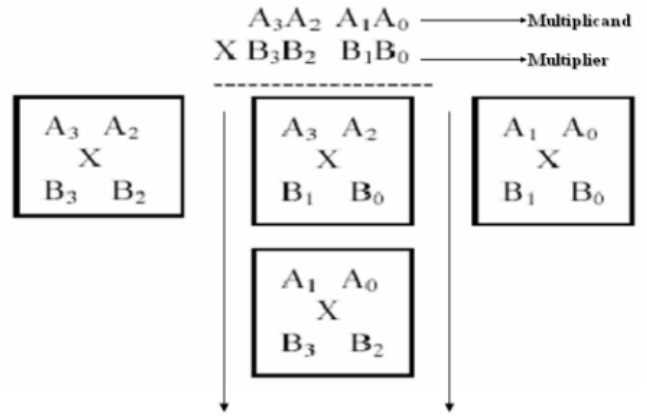



Fig (2): Vedic Multiplier For 4x4 Bit




In two equal portions, divide the total number of bits in the inputs. 51 A and B are equal to A3A2A1A0 and B3B2B1B0, respectively, and let's examine 4x4 bit multiplication. These are S7 S6 S5 S4 S3 S2 S1 S0, the output lines for the multiplication result. Using the terms "A3 A2" & "A1 A0" for A and "B3 B2" & "B1 B0" for B, let's split A and B into two components. We may create the 4x4 bit multiplication structure depicted in the image by applying the fundamentals of vedic multiplication, taking two bits at a time, and employing a 2-bit multiplier block. "A1 A0" and "B3 B2" are the initial 2x2 multiplier inputs. With inputs "A3 A2" & "B1 BO" and "B3 B2," the middle one displays a two-by-two bit multiplier. Thus, 8 bit S7 S6 S5 S4 S3 S2 S1 S0 is the result of multiplication in the end. The many architectural block diagrams used to create the 4x4 Vedic multiplier and the corresponding delays are displayed here. The 2x2 multiplier is used in this design to first produce partial products, which are then added to get the desired outcome. We have covered a number of methods in these architectures for adding these partial products and calculating delays for each architecture.

International Scientific Journal of Engineering and Management
Volume: 03 Issue: 04 | April – 2024
An International Scholarly || Multidisciplinary || Open Access || Indexing in all major Database & Metadata
ISSN: 2583-6129
DOI: 10.55041/ISJEM01526

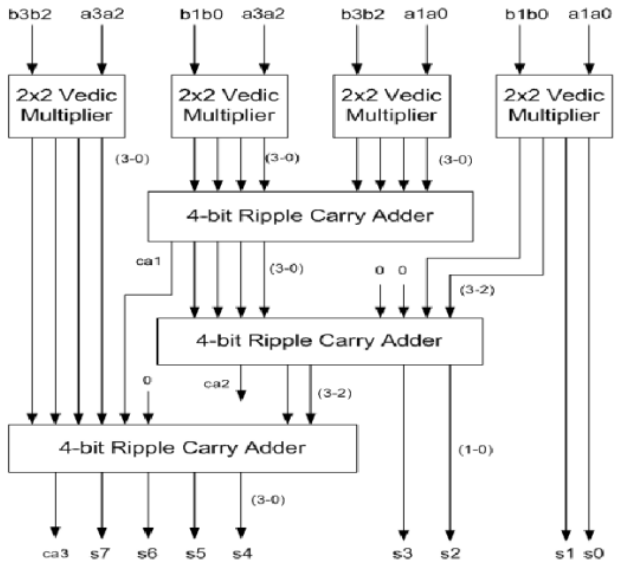
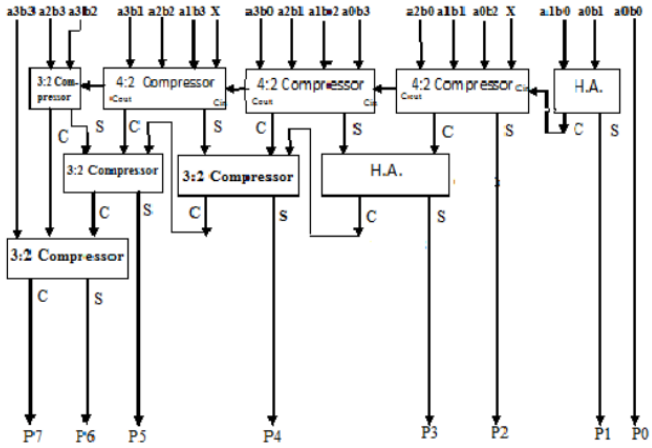



Fig (3): Existed Vedic Multiplier

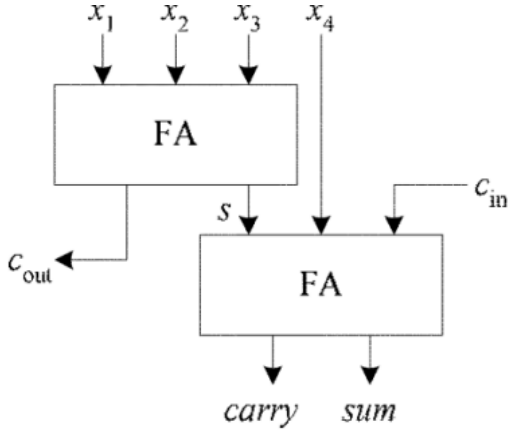
A compressor is a type of combinational circuit that may add four or more bits at once. A compressor works well in place of several half adders and full adders. Because of this, its main advantages are faster processing times for processes and lower critical path latency when using less power.

## II. COMPRESSOR BASED VEDIC MULTIPLIER



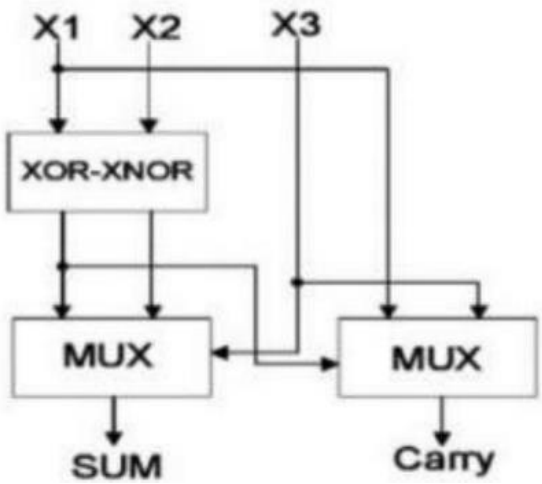

*4:2 Compressors:*

Two complete adders connected in series make up the 4:2 compressors. We use a compressor adder instead of another adder since it has less carry propagation. A modern digital circuit that runs quickly and requires minimum gate design is a compressor. It is called as it reduces the four patial products to two. While the input cin is the output from the adjacent previous stage compressor, the output ae cout is the output to the next step compressor. The analogous circuit of a 4:2 compressor with a complete adder is shown in Figure. The compressor in the illustration is made up of two full adders connected in series.




*3-2 Compressor:*

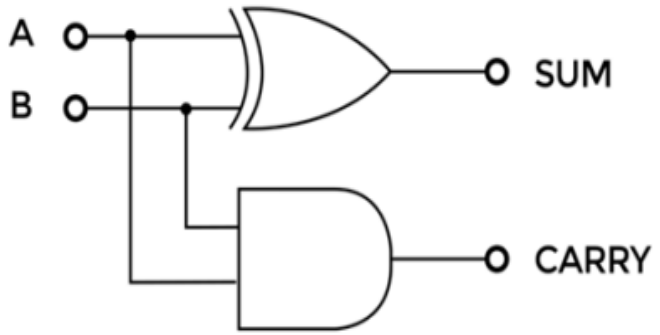
A basic 3-2 compressor is a single bit adder circuit with two outputs and three inputs (as in a complete adder). The proposed hybrid architectures efficiently use both XOR and XNOR logic to reduce latency.



International Scientific Journal of Engineering and Management
Volume: 03 Issue: 04 | April – 2024
An International Scholarly || Multidisciplinary || Open Access || Indexing in all major Database & Metadata
ISSN: 2583-6129
DOI: 10.55041/ISJEM01526

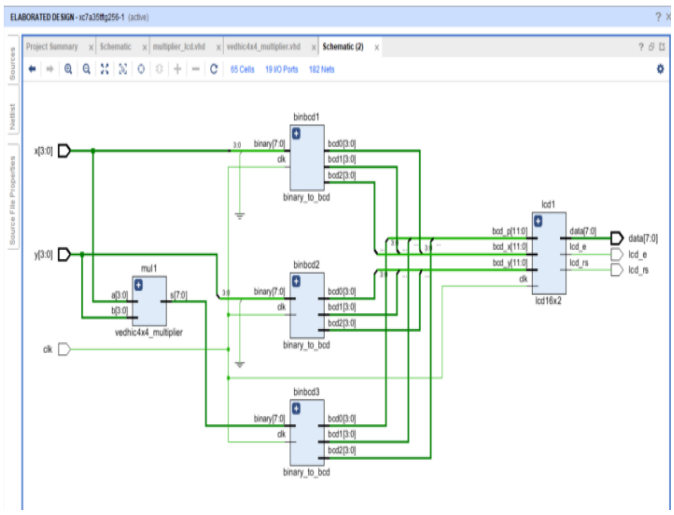
*Half Adder:*



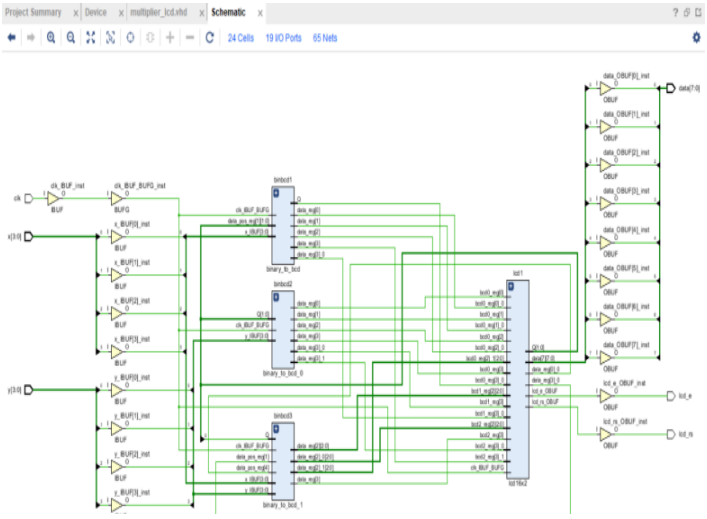

A digital logic circuit known as a half adder is used to add two single-bit binary integers in binary. It has two outputs, SUM and CARRY, and two inputs, A and B. Indicating if there was a carry-over from the addition of the two inputs, the SUM output is the least significant bit (LSB) and the CARRY output is the most significant bit (MSB) of the result.

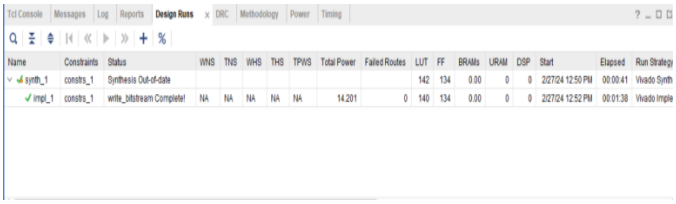
## III. RESULTS AND CONCLUSIONS:

The code for 4x4 vedic multiplier need some files that should be added. Those files are 4:2 compressor,3:2 compressor, half adder. These code are driven into FPGA board to LCD.LCD which contains the code of LCD display i,e., how the data should be displayed on it.

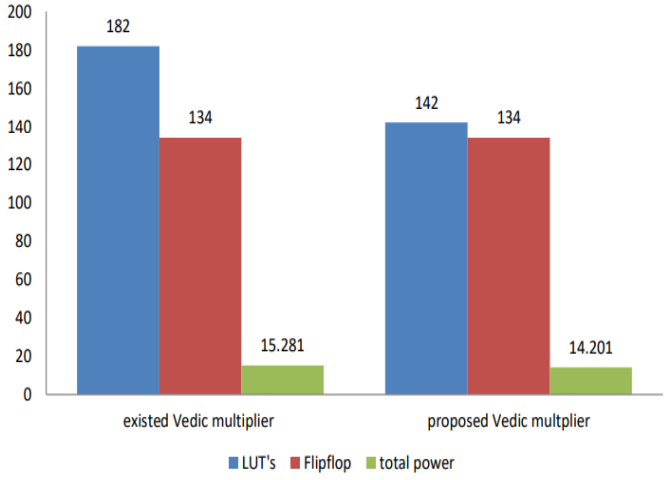


The above figures are schematic and table that contains number of LUTs and power of Existed Vedic Multiplier.





The above figures show that schematic and total power, no. of LUTs for proposed Vedic multiplier.



ISSN: 2583-6129
DOI: 10.55041/ISJEM01526

## IV. CONCLUSION:

The below graph shows that comparison between the existed Vedic multiplier and proposed Vedic multiplier. Here, we can conclude that the total power and luts are less in the proposed Vedic multiplier. Hence, power consumption is less and space efficient.

**REFERENCES**

[1] Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja,"Vedic Mathematics or Sixteen Simple Mathematical formula form the veda ,delhi (1965)",motilal Banarsidas, Varanasi, India, 1986.

[2] Vitthal B. Jadhav, Charan Lal "Demystifying Speed Mathematics" First Edition May 2016.

[3] Sayali Shembalkar, Samiksha Dhole, Tirupati Yadav, Prasheel Thakre, " Vedic Mathematics Sutras -A Review", International Conference on Recent Trends in Engineering Science and Technology (ICRTEST 2017), ISSN: 2321- 8169, Volume: 5 Issue: 1( Special Issue 21-22 January 2017),pg-148 -155.

[4] Anuva Das, Mrs. J. K. Kasthuri Bha, "Design Optimization of Vedic Multiplier using Reversible Logic" International Journal of Engineering Research & Technology (IJERT), Vol. 3 Issue 3, March – 2014, ISSN: 2278-0181.

[5] B.Ratna Raju, D.V.Satish, "A High Speed 16*16 Multiplier Based On Urdhva Tiryakbhyam Sutra", International Journal of Science Engineering and Advance Technology, IJSEAT, Vol 1, Issue 5, October – 2013.