Design and Implementation of an Efficient Quantum Cost Optimized Full Adder Using Reversible Logic Gates

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Abstract**—**In the context of modern Very Large-Scale Integration (VLSI) technology, information loss has been a major concern. Logic gates (LG) such as AND, OR, and NOT have been found to result in information loss during their operations. To address this issue, reversible LGs have been created. The development and implementation of a high-speed, efficient full adder circuit employing reversible LGs like Feynman, Toffoli, and Peres gates. The design aims to improve computational and thermal efficiencies. The circuit refarding quantum costs (QC), garbage outputs, and ancillary inputs. The implemented the suggested design in Verilog and verified the entire adder's functionality and efficiency through simulations using the Xilinx Vivado and Xilinx ISE tools. The circuit has a quantum cost of 10 with two outputs of useless and one auxiliary input, according to the researchers, highlighting its opportunities for usage in quantum computing applications and low-power (dec 84%), high-performance computing systems.

Keywords— Reversible logic, Feynman gate, Toffoli gate, Peres gate, Full Adder, Verilog, Quantum Cost.

I. INTRODUCTION

In recent years, the field of VLSI has experienced tremendous growth, resulting in higher circuit density and computational power. Nevertheless, this progress has also led to substantial problems with power dissipation and heat generation. The main reason for energy loss in traditional digital circuits is the irreversible nature of standard logic gates (LGs), namely AND, OR, and NOT. The main problem with these gates is that they do not conserve the input information after the computation.

Reversible logic offers a unique mapping within inputs and outputs, allowing the original inputs to be recovered from the resulting outputs. This characteristic provides that absence of details is discarded while the computation process. Since information loss is minimized, power dissipation is also reduced. Consequently, reversible logic has become a crucial concept in the creation of energy-efficient VLSI circuits, nanotechnology systems, and quantum computing technologies.

A full adder is an elementary arithmetic circuit that has many applications in digital systems for binary addition. A reversible full adder circuit design utilizing reversible LGs can greatly improve energy efficiency without compromising accuracy. In this study, a bidirectional full adder circuit is proposed in light of Feynman, Toffoli, and Peres gates. The proposed circuit aims to minimize the amount of ancilla inputs, eliminate unnecessary outputs, and reduce the overall QC to improve circuit efficiency.

II. LITERATURE SURVEY

The idea of reversible logic has garnered a much of research intrigue lately due to its potential for creating circuits that are quantum compatible, ultra-low power, and highly efficient. Due to the inherent irreversibility of conventional logic circuits, the output does not retain enough information to reconstruct the input. Consequently, every bit of information lost during computation adds to the dissipation of energy. [1] Zeliang et al. proposed an efficient full adder architecture using a newly developed Tuned Fredkin Gate (TFG). The design focuses on improving the performance of reversible circuits while reducing QC and garbage outputs. [2] Chacko and Whig designed a low-delay subtractor using MIG and COG reversible LGs. Their approach aims to enhance computation speed and optimize circuit performance in reversible computing systems.

[3] Bhuvaneswary and Lakshmi presented the development and optimization of reversible look-ahead bear adders and bear save adders. Their work emphasizes improving efficiency and reducing computational delay in reversible arithmetic circuits. [4] Kalita et al. explored the development of adder circuits employing reversible LGs. The study focuses on improving power efficiency and minimizing unnecessary outputs in reversible adder implementations.

[5] Chiwande and Dakhole developed a low-power full adder using reversible logic techniques. Their design aims to decrease energy consumption and enhance the efficiency of

digital circuits. [6] Pujar et al. proposed an energy-efficient reversible logic-based complete adder. The design emphasizes reducing power dissipation and optimizing parameters such as QC and delay.

[7] Hashemi et al. designed efficient reversible adders utilizing Quantum-dot Cellular Automata (QCA). The study analyzes the performance and efficiency of reversible adder structures in nanoscale computing environments. [8] Thapliyal and Ranganathan focused on the development of reversible sequential circuits while optimizing key parameters such as QC, delay, and trash outputs. Their study contributes to improving the efficiency of reversible circuit designs.

[9] Singh and Rai presented the Verilog implementation of a full adder based on reversible LGs. The study demonstrates how reversible designs can be implemented using hardware description languages for digital systems. [10] Singh et al. presented a novel development for reversible memory elements with the objective of reducing delay and QC. Their work concentrates on enhancing the efficiency and performance of reversible computing components used in advanced digital and quantum systems.

Even though earlier reversible adder designs have made a substantial contribution to the field, they still have a number of shortcomings, including high QC, excessive garbage outputs, increased delay, scalability, and hardware inefficiency.

III. PROPOSED MODEL

The proposed circuit consists of one 2x2 Feynman gate, one 3x3 Toffoli gate, and one 3x3 Peres gate. The suggested circuit's QC is 10. Two trash outputs and one ancilla input are generated. The fig.1 represents the proposed circuit diagram. Here, the Feynman gate is used as an EX-OR gate, denoted by the S0 port, and produces the garbage output 'GP1'. The Toffoli gate is used as an AND gate, denoted by the S1 port, and produces two outputs, which are further taken as inputs to the Feynman gate 'A' and 'B'. The Toffoli gate requires an ancilla input '0' along with the two inputs 'A0' &'B0'. The Peres gate takes the outputs of the Feynman and Toffoli gateway, along with the third input The Peres gate presents the required sum and Cout values of the adder while also producing a garbage output denoted as GP2.
The suggested complete adder is less expensive than the current design, with a fundamental cost of 10. Additionally, it uses fewer ancilla inputs and produces fewer trash outputs. The circuit becomes increasingly appropriate for low-power VLSI systems and quantum-computer applications as the overall cost of reversible-logic implementation decreases.

The design is further validated through simulation and implementation on vivado platform, demonstrating correct operation and improved hardware efficiency compared to the existing system.

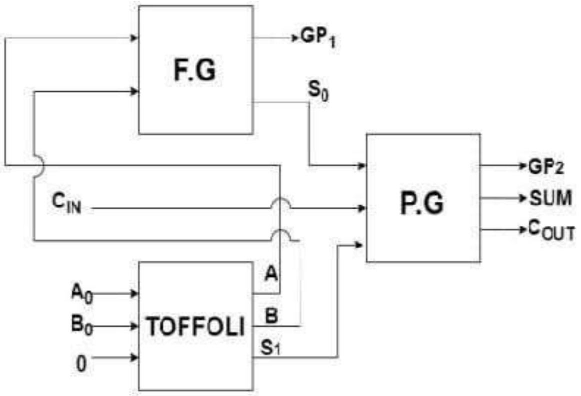

Fig.1. Proposed Full adder circuit using reversible gate

IV.REVERSIBLE LOGIC GATES

Traditional LGs are observed to have the inherent property of losing information during the computation process. Such loss of information results in the dissipation of extra power as well as the production of heat. Such an issue is observed with the increase in complexity in the circuit. The problem is solved with the introduction of reversible LGs that do not have the property of losing information during the computation process.

A LG can be considered to be reversible if it has the same number of input lines as it has output lines. Therefore, the input values can be specially established by the output values. This feature of the LG helps to make the computation process information-lossless. This LG characteristic contributes to a better degree of circuit power dissipation reduction.
However, there is one constraint associated with reversible logic as well: there cannot be any fan-out or feedback in the circuits. Although certain limitations exist, the advantages of reversible LGs in improving power efficiency and computational speed are significant. Due to these benefits, they are widely applied in areas such as quantum computing, optical computing, and energy-efficient VLSI circuit design.
In this proposed system, Feynman, Toffoli, and Peres gates are employed due to flexibility in operation and low QC. These types of LGs are useful in the efficient implementation of arithmetic operations.

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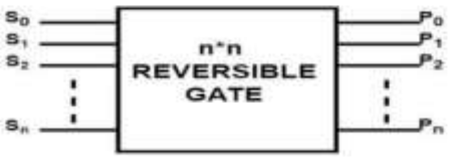

FIG.2. BASIC REVERSIBLE GATE

Fig.2 represents the basic reversible gate symbol. The three important matrices in design of reversible LGs are
(i) Quantum cost (QC)- QC is described as the total amount of Elementary Quantum Gates which are needed to realize a particular reversible LG.

(ii) Garbage outputs- They are unwanted outputs generated by reversible LGs but also equally important to maintain reversibility nature of reversible LGs.
(iii) Ancilla input- It can be defined as the quantity of inputs sustained constant at 0 or 1 for synthesizing the given logical function.

These three criteria determine the efficiency of reversible LGs.

USES:

1. **Quantum computing** – Reversible LGs act as a crucial and form a fundamental base in quantum computing circuits due to the reversible nature of quantum operations.
2. **Low-power computing** – Reversible gates can potentially reduce energy consumption by minimizing information loss.
3. **Cryptography** – Reversible LGs can be used for the purpose of designing secure cryptographic algorithms.

ADVANTAGES:

1. **Energy Efficiency –** Reversible LGs help reduce energy dissipation because they preserve information during computation, preventing information loss**.**
2. **Compatibility with Quantum Computing –** Reversible LGs are fundamental components in quantum computing, as quantum operations require reversible transformations.
3. **Error correction** - Reversible LGs can be helpful in error correction by allowing the recovery of input states from output states.

Several reversible LGs which has been implemented in this design are as follows

A. Feynman Gate (FG):

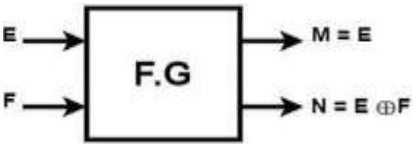

Fig.3. Feynman gate

The Feynman gate is a widely used reversible LG that has two input terminals and two output terminals, and it is commonly represented as FG.
In the given above Fig.3, the terminals E and F represents the two input ports and the terminal M and E represents the two output ports. The output can be represented using the expression**: M=E, N=E⊕ F.**
The Feynman gate has a QC of 1. It can also function as an XOR gate, where the output at the N terminal provides the required XOR result.
Table 1 below shows the truth table of the FG.

TABLE.1.: TRUTH TABLE OF THE FG

INPUT		**OUTPUT**	
E	F	M	N
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

B. Peres Gate (PG):

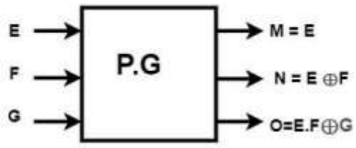

Fig.4. Peres gate

The PG is an important reversible LG that consists of three input terminals and three output terminals, and it is commonly denoted as PG.
In the given above Fig.4, the terminals E, F & G represents the three input ports and the terminal M, N & O represents the three output ports. The output can be represented using the expression: **M= E, N = E⊕ F** and **O=E.F⊕ G.**
The QC for Peres gate is 4. It is highly used for the purpose of designing of adder circuits and it can also be used as a AND gate. Putting G=0, the PG outputs will be altered as: M=E, N=E⊕ F and O=E.F and O terminal will give us the desired AND gate output.
Table 2 below displays the truth table of the PG.

TABLE.2.: TRUTH TABLE OF THE PG

INPUT			**OUTPUT**		
E	F	G	M	N	O
0	0	0	0	0	1
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1

C. Toffoli Gate (TG):

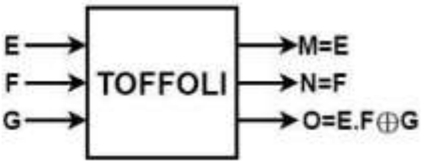

Fig.5. Toffoli Gate

The Toffoli gate is a reversible LG that has three input terminals and three output terminals.
In the given above Fig.5, the terminals E, F & G represents the three input ports and the terminal M, N & O represents the three output ports. The output can be represented using the expression:
M=E, N=F and **O=E.F⊕ G**.
The Toffoli gate has a QC of 5. It can also be used to implement an AND gate. When the input G=0, the outputs of the Toffoli gate change accordingly, and the output at terminal O provides the required AND operation.

Table 3 below shows the truth table of the TG.

TABLE.3.: TRUTH TABLE OF THE TG

INPUT			**OUTPUT**		
E	F	G	M	N	O
0	0	0	0	0	0
0	0	1	0	0	1
0	1	1	0	1	1
0	1	1	0	1	1

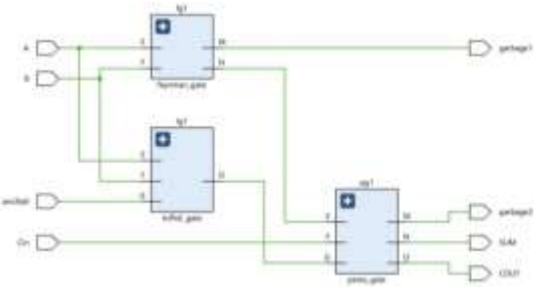

Fig.6. Schematic Diagram of Efficient QC Optimized Full Adder using Reversible LGs

V. *SIMULATION RESULTS*

The proposed design was simulated using Xilinx Vivado HLS version 2018.2 and Xilinx ISE 14.7 tools. The correctness and performance of the design were validated through simulation results obtained from four different test cases. The 1-bit full adder uses A, B, and Cin as input ports, while SUM and Cout represent the output ports. Figures 7 to 10 illustrate the simulation results of the presented circuit. The table.4 demonstrates the truth table of the presented design, which represents the inputs and outputs.

TABLE.4.:TEST CASE RESULT IN SIMULATION

TEST CASE	**A**	**B**	**Cin**	**SUM**	**Cout**
1	1	0	0	1	0
2	1	0	1	0	1
3	1	1	0	0	1
4	1	1	1	1	1

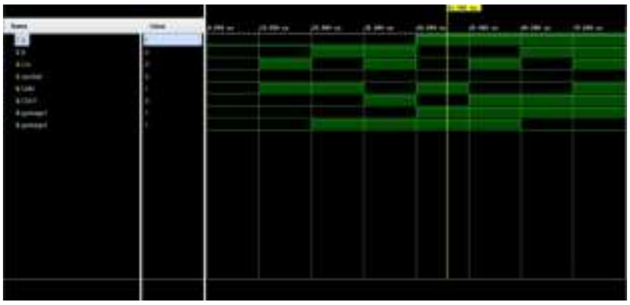

Fig.7. Simulation outcome for the first test case

Fig.8. Test case 2's simulation outcome

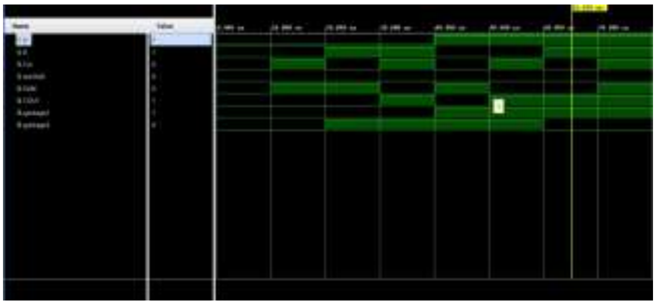

Fig.9. Simulation outcome for Test Case 3

Fig.10. Test case 4 simulation outcome

TABLE.5.: COMPARATIVE STUDY WITH EXISTING MODEL

PARAMETERS	**QUANTUM COST**	**GARBAGE OUTPUTS**	**ANCILLA INPUTS**	**NUMBER OF GATES**	**TRLIC**
[1]	15	2	1	2	20
[2]	16	3	2	2	23
[3]	12	3	2	3	20
PROPOSED	**10**	**2**	**1**	**3**	**16**

VI. CONCLUSION

This work presents the design and implementation of a full adder optimized for QC using reversible LGs. Using Feynman gates, Toffoli gates, and Peres gates, the proposed design was able to minimize the overall QC, garbage outputs, and ancilla inputs in comparison with conventional reversible adder designs. The optimized design was able to improve the hardware efficiency, allowing it to be used minimal-power VLSI circuits and upcoming solutions in quantum computing.

The results verified the proposed design's effectiveness in the application of reversible logic in arithmetic circuit design.

VII. FUTURE SCOPE

Future research can apply this method to the development of more sophisticated arithmetic and logic circuits, such as multipliers, arithmetic logic units, and signal processing circuits.

Optimization of the reversible architecture can be used to further the development in the fields of quantum computing, nanotechnology, and energy-saving digital systems.

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