

TITLE: DESIGN OF 4-BIT MULTIPLIERS USING MODIFIED GATE DIFFUSION INPUT TECHNOLOGY FOR LOW POWER APPLICATIONS

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Abstract - Multipliers are widely used in digital circuits for countless arithmetic operations and are critical components in many very large scale integration systems. The multiplication process is one of the basic processes in digital equipment, and hardware multipliers play a key role in facilitating efficient data processing and fast computing. The demand for multipliers that are characterised by low energy consumption and high performance has stimulated the development of a variety of design methods, with particular emphasis on surface and energy efficiency. In this research we introduce a modified gate-diffusion input (MGDI) cell architecture for a 4-bit field multiplier that shows a higher energy efficiency than traditional designs of multipliers. The MGDI-based multiplier achieves a significant reduction in energy consumption (1.109861 mW) while maintaining the necessary operational efficiencies. The 4-bit MGDI multiplier is carefully designed using Tanner EDA tools, and extensive simulations have been performed to demonstrate its performance.

Key Words: *Modified Gate Diffusion Input (MGDI), Low Power, 4-Bit Multiplier, Transistor Count, Time delay.*

I.INTRODUCTION

Many important works clarify the various approaches to multiple optimization. The 3-bit encoding technique optimized for parallel multipliers using two-sided complement representation demonstrated a latency of less than 5.7 ns for the 8x8-bit multiplier using CMOS SCN technology. The reconfigurable 8x8 wall wart multiplier, which was created by combining CMOS and GDI technologies in the 180 nm process, offered significant improvements in structural homogeneity and energy efficiency. The versatility of gate-diffusion input (GDI) technology has been demonstrated by the reduction in power consumption and number of transistors resulting from its use in the 4-bit field multiplier. Other advances included the optimization of the power delay product by integrating a 10-transistor (10T) full-array accelerator in a 4-bit field multiplier. On the other

hand, the combination of lowenergy design techniques has underlined the importance of energy efficient design in portable devices. The propagation delay, power dissipation and power delay product have all been significantly reduced by 4x 4-bit. Dadda multipliers using 10T full amplifiers. High speed and low power performance has been achieved using Vedic mathematical concepts in 4-bit Vedic multipliers based on GDI. At the same time, a new low-power full-array amplifier combining pass-through logic (PTL) and GDI has demonstrated improved energy efficiency in arithmetic operations. Finally, the area, energy consumption and time-to-life gains were obtained by the Radix-8 high-speed binary multiplier using Urdhva-Tiryakbhyam and GDI techniques. These developments underline the need for modern design to strike a careful balance between power, speed and accuracy. In addition, FPGA implementations of Vedic multipliers highlight the benefits of parallelism and pipelining in achieving higher throughput and lower latency. 4-bit multipliers use reversible logic gates to reduce the production of heat and to increase energy efficiency. For 8-bit multipliers, a comparison between CMOS and FinFET technology has shown that FinFET devices have a lower leakage energy and a higher speed of operation. In field multipliers, GDI has successfully reduced transistor count and energy consumption. Wallace tree multipliers have improved speed and energy efficiency by making partial reductions more effective. Low power multiplier designs, which are ideal for portable devices, have been made possible by the logic of the transmission gate.

II. OVERVIEW OF FULL ADDER

A full-length adder is a logical circuit that requires three one-bit binary digits to accomplish the addition function. When two input numbers are added together, full adders generate a carry-over output. It can function both separately and in conjunction with other full adders. Three one-bit binary values (C, A, and B) are processed by the full-adder circuit to yield two one-bit binary outputs: the sum (S) and the carry (C1). In a cascade design, the carry-over to the full-adder circuit originates from the carry-out from the preceding circuit. The fundamental design of the entire adder circuit is based on the truth table, and the and the output equations are represented by:

$$(1) S = X \text{ xor } Y \text{ xor } Z$$

$$(2) C_{out} = (X \text{ and } Y) \text{ or } (Y \text{ and } Z) \text{ or } (Z \text{ and } X)$$

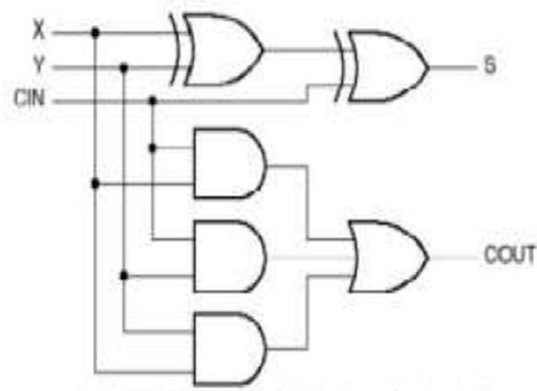


Fig. 1. Diagram of a 1-bit full adder block.

III. DESIGN METHODOLOGY

MGDI is based on the use of basic cell structures. At first glance, the core cell is similar to a traditional CMOS inverter. However, there is an important difference.

1. Common gate inputs for both NMOS and PMOS transistors. It is represented by the letters p (PMOS Source and drain input) and n (nmos Source and drain input) are three inputs defined by the MGDI cell.
2. In CMOS and traditional pass-through transistor logic(PTL) implementations, most of these functions are very complex, but multi-gate differential logic (MGDI) techniques are very simple and require only two transistors to perform each function.

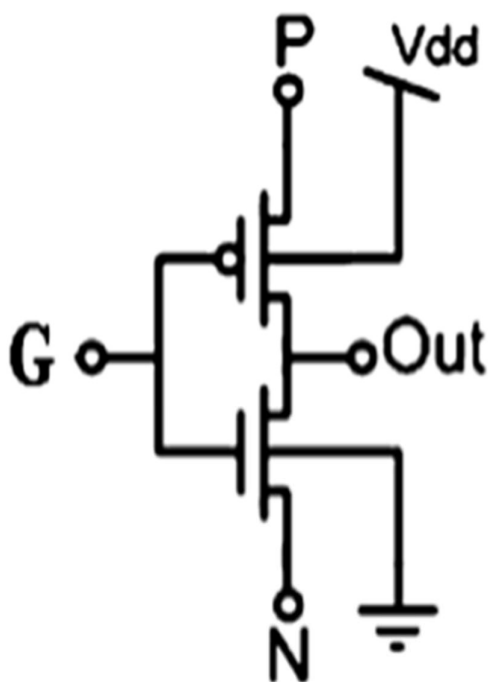


Fig. 2. MGDI basic cell

3. A 4x4 matrix multiplier has been developed using 16 AND gates and 3 4-bit full complement gates. The accompanying figure shows a schematic representation of a 4x4 matrix multiplication factor. This design is characterised by a smaller number of transistors and a significantly lower energy consumption.

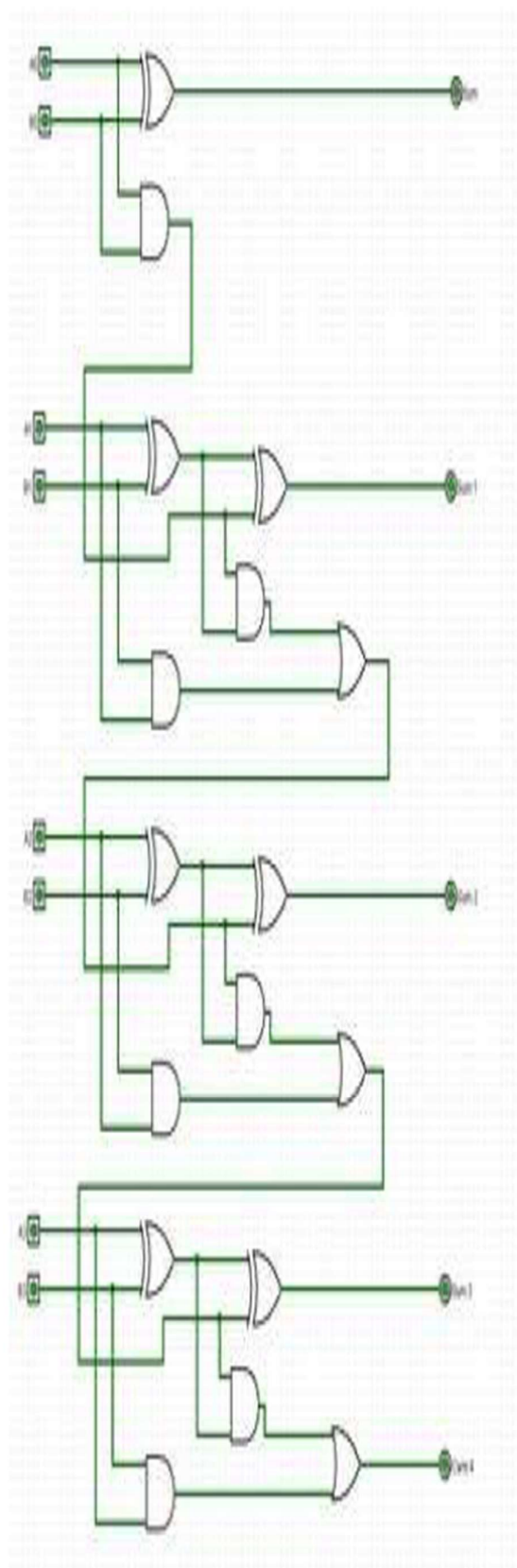


Fig. 3. Diagram of a 4-bit full adder block.

IV. PERFORMANCE PARAMETERS OF FULL ADDER

A. Power Dissipation

Power dissipation pertains to the quantification of energy utilized and subsequently "lost" by the full adder during its operational phases. This energy loss manifests through two principal mechanisms:

Static Power: This phenomenon transpires when the adder remains in a non-switching state yet still consumes energy owing to leakage currents (even in instances where transistors are not activated). **Dynamic Power:** This phenomenon occurs during the state transitions of the adder, such as when executing the addition of two numerical values. It is attributable to the necessity for internal capacitors to undergo charging and discharging processes each time the adder completes a computational task.

B. Propagation Delay

This indicates that the circuit spreads faster than it takes for the input signal to reach 50% of the exit level.

C. Power-Delay Product (PDP)

The Power-Delay Product integrates power dissipation and propagation delay into a singular quantitative measure. This metric elucidates the energy expenditure of the adder per operational cycle as well as the temporal duration required to execute that operation. A reduced PDP is advantageous as it performance and energy efficiency.

V. SIMULATION RESULTS AND DISCUSSIONS

The modified full adder is constructed in the same way full adder. It contains arithmetic adder circuit and full adder circuit. In the modified full adder, all of the AND gates are replaced with EX-OR gates.

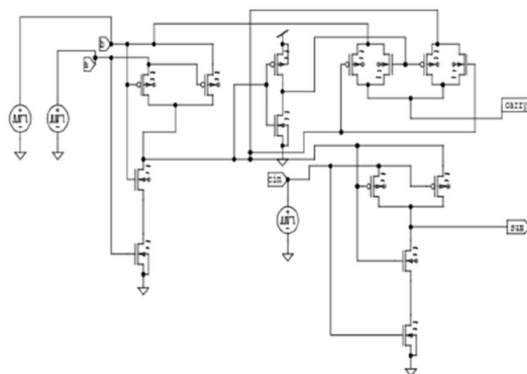


Fig. 4. 1-bit circuit diagram for normal GDI

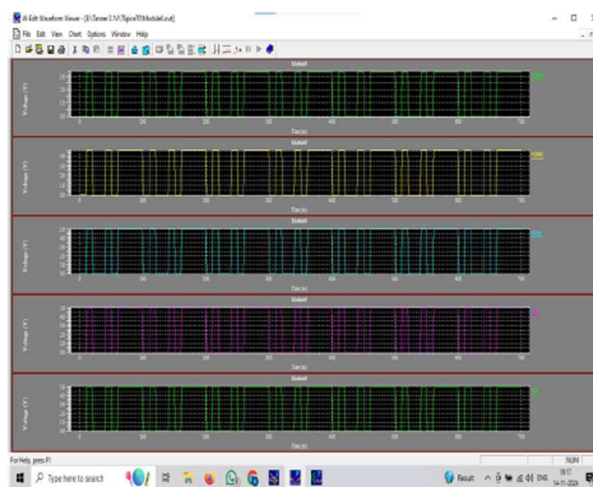


Fig. 5. Output waveform of GDI 1-bit full adder

This Fig.4 and Fig.5 describes the construction of a single bit full adder circuit that uses MOSFETs to enhance the adder's performance in terms of 14 transistors are used for power and leakage. The Fig.4 shows 4T XOR gate is used in the construction of this cell. It is the fundamental component of a complete adder cell and produces the adder cell's fundamental addition action. It functions similarly to a single half adder cell. Two 4T XOR gates were employed in the 14T complete adder cell. XOR gates typically require

eight MOSFETs to function properly, however today we have a variety of topologies. To improve circuit density, we have employed a 4T XOR gate in this instance. Both total leakage and the size of the entire adder are decreased with the use of this XOR gate.

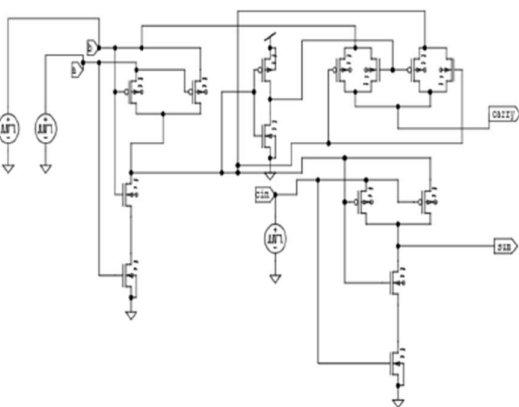


Fig. 4. 1-bit circuit diagram for normal GDI

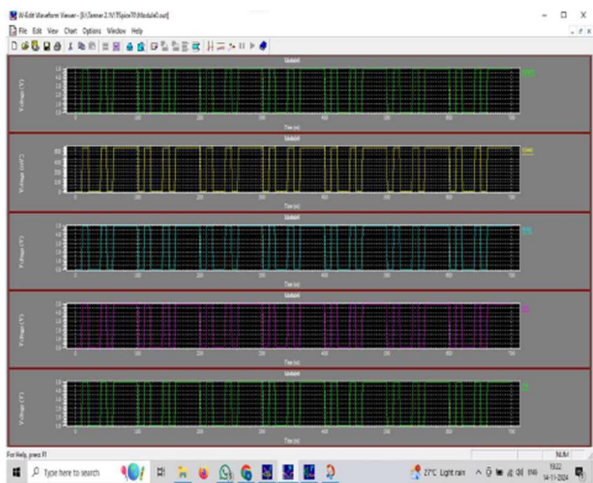


Fig. 7. Output waveform of MGDI 1-bit full adder

The Fig. 6 and fig. 7 shows the design of a single-bit full adder circuit is optimized using a 10-transistor (10T) configuration to enhance performance and efficiency. This design employs a 4T XOR gate as the core component for generating the sum output, significantly reducing the transistor count compared to traditional XOR implementations. By integrating the XOR gate with efficient pass transistor logic for carry generation, the circuit achieves the required

functionality with only 10 transistors. This compact design reduces power consumption, leakage, and overall circuit size while maintaining reliable operation. The 10T full adder is particularly advantageous for low-power, high-density applications where minimizing transistor count and enhancing performance are critical. Compactness, establishing it as an exemplary selection for contemporary digital circuit design endeavors.

TABLE II. COMPARISON BETWEEN 4-BIT FULL ADDERS

Types of logic	Conventional logic 4-Bit Full Adder	GDI 4-Bit Full Adder	MGDI 4-Bit Full Adder
No. of transistors	416	56	40
Power Consumption(mW)	32.81	2.59117	1.108961
Delay (s)	0.39	0.31	0.12
Power-Delay Product (PDP)	12.7959	0.8032	0.133075

TABLE.II shows the MGDI 4-bit full adder demonstrates considerable advancements relative to the GDI 4-bit full adder concerning operational efficacy and efficiency. Furthermore, the MGDI adder exhibits a lower power consumption, measuring at 1.108961 mW in contrast to 2.59117 mW for the GDI, rendering it more appropriate for applications that are sensitive to power usage. In addition, the latency associated with the MGDI 4-bit full adder is significantly minimized at 0.12 s, compared to 0.31 s for the GDI, which suggests enhanced processing speed and superior performance for high-velocity digital systems. In

summary, the MGDI 4-bit full adder represents more effective and high-performance alternative for contemporary digital circuit implementations.

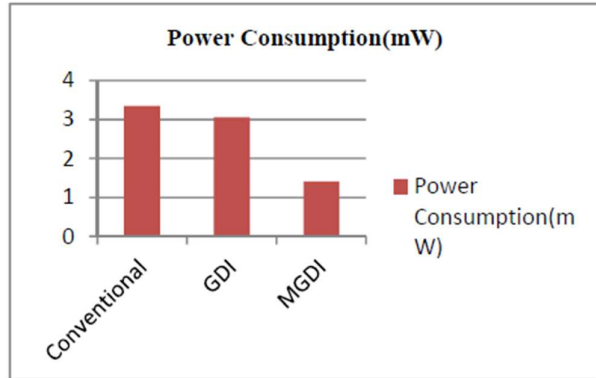


Fig.10. Comparison of power consumption (mW)

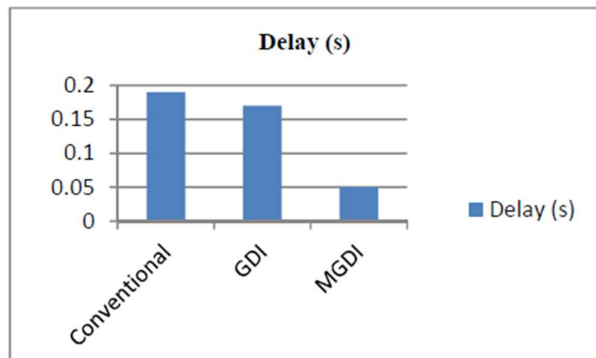


Fig.11. Comparison of Delay(s)

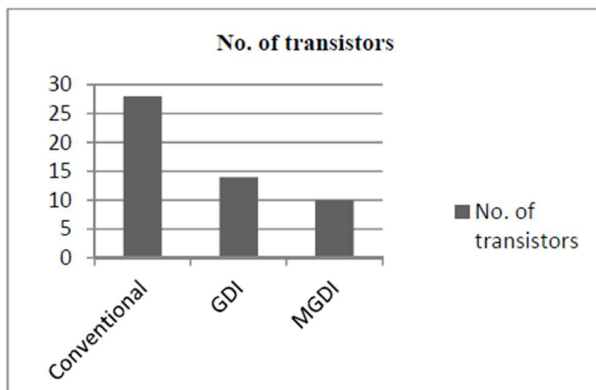


Fig.12. Comparison of No. of transistors

VI. RESULTS AND CONCLUSION

When compared to conventional CMOS designs, the VLSI domain's implementation of a 4-bit multiplier using MGDI(Modified Gate Diffusion Input) technology shows low power consumption and Time delay. This makes MGDI a great option for low.

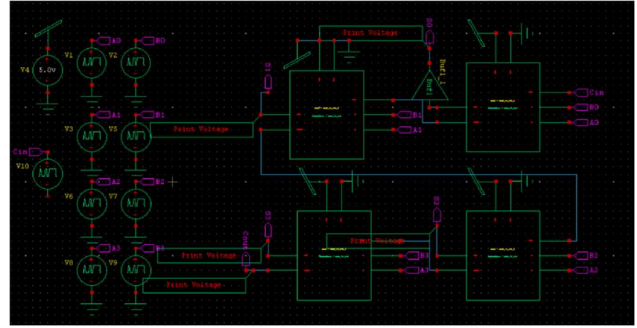


Fig.13. Schematic Diagram

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General options:
  threads = 1

Device and node counts:
  MOSFETs - 60
  MOSFET geometries - 5
  Voltage sources - 10
  Subcircuits - 5
  Model Definitions - 6
  Computed Models - 2
  Independent nodes - 31
  Boundary nodes - 11
  Total nodes - 42
*** 1 WARNING MESSAGE GENERATED DURING SETUP

Power Results

VV1 from time 0 to 2e-008
Average power consumed -> 3.989790e-008 watts
Max power 5.995817e-006 at time 1.10343e-008
Min power 2.051636e-011 at time 2e-008
    
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Fig.14. Output(1)

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VV2 from time 0 to 2e-008
Average power consumed -> 2.184217e-011 watts
Max power 2.605869e-008 at time 1.11937e-008
Min power 2.912189e-012 at time 1.81278e-008

VV3 from time 0 to 2e-008
Average power consumed -> 0.000000e+000 watts
Max power 0.000000e+000 at time 0
Min power 0.000000e+000 at time 0

VV5 from time 0 to 2e-008
Average power consumed -> 2.869451e-006 watts
Max power 1.165397e-004 at time 1.025e-008
Min power 0.000000e+000 at time 1.1e-008

Parsing 0.08 seconds
Setup 0.05 seconds
DC operating point 0.02 seconds
Transient Analysis 0.03 seconds
Overhead 0.26 seconds
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Total 0.44 seconds
    
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Fig.15. Output(2)

It simulates in Tanner EDA; MGDI cells replace CMOS logic. It targets at low-power VLSI: IoT, portable processors.

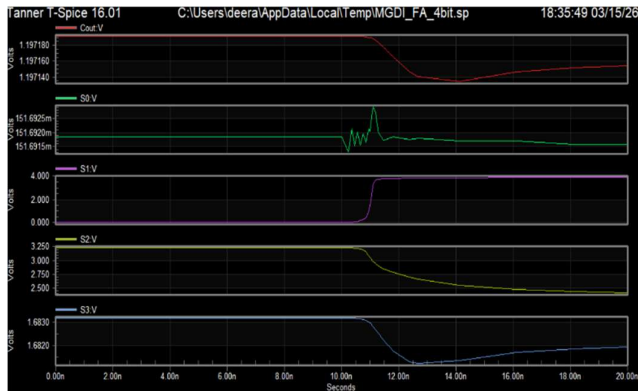


Fig.16. Waveforms

Low power, high-efficiency VLSI circuits, especially for applications like mobile processors, Internet of Things chips, and portable VLSI systems where reducing power consumption and chip space is essential. As a result, when compared to conventional logic, the proposed MGDI architecture achieved notable improvements, reducing power consumption by 57% and time delay by 73%. These findings demonstrate how MGDI technology can be used to improve efficiency in circuits that need to process information quickly and with low power consumption., and it is a good option for next-generation, energy-conscious VLSI designs.

REFERENCES

[1] SanchitaTongya, Rahul Sharma, and GajendraSujediya, "Design and Analysis of 4-Bit and 8-Bit Multiplier Using GDI and CMOS Technology," International Journal of Innovative Research in Science, Engineering and Technology, vol. 8, no. 8, pp. 8480–8485, Aug.2019, doi: 10.15680/IJRSET.2019.0808021

[2] Bini Joy, N. Akshaya, and M. SathiaPriya, "Design of Multiplier Using GDI Technique," International Journal of Advanced Research in Science and Engineering, vol. 4, Special Issue 2, pp. 373–375, Feb.2015.

[3] Vinothkumar K., Kavitha B., Keerthana A., and Kowsalya Devi V., "Full Adder Design Implementation by Using Transistor and XNOR

Gate," International Research Journal of Engineering and Technology, vol. 7, no. 9, pp. 882–883, Sep. 2020.

[4] Saranya L., AarshaNath, Kavitha M., and Karthika K., "Power Optimization in 10T Full Adder for 4-Bit Array Multiplier," International Journal of Innovative Technology and Exploring Engineering, vol. 8, no. 6S, Apr. 2019.

[5] K. Ragini and B. Neerajakshi, "Design and Implementation of 4×4 Bit Multiplier Using Dadda Algorithm," Journal of Emerging Technologies and Innovative Research, vol. 6, no. 6, Jun. 2019.

[6] K. Nishanth Rao, D. Sudha, Osamah Ibrahim Khalaf, GhaidaMuttasherAbdulsahab, Aruru Sai Kumar, S. Siva Priyanka KhmaiesOuahada, and Habib Hamam, "A Novel Energy-Efficient 4-Bit Vedic Multiplier Using Modified GDI Approach at 32 nm Technology," Heliyon, vol. 10, pp. e31120, May 2024, T. Nirmalraj, S. K. Pandiyan, Rakesh Kumar Karan, R. Sivaraman, and RengarajanAmirtharajan, "Design of Low-Power 10-Transistor Full Adder Using GDI Technique for Energy-Efficient Arithmetic Applications," Circuits, Systems, and Signal Processing, vol. 42, pp.3649–3667, Jan. 2023

[7] J. Aditya, N. Reddy, G. S. Krishna, and P. Bikki, "Novel High-Speed Vedic Multiplier," ResearchGate, Mar. 2024.

[8] Prabhakar, A. S. N. Sambhi Reddy, B. Durga Pradesh, Ch. Shivani, and Ch. Rakesh, "Implementation and Validation of 16-Bit RISC Processor Using Vedic Mathematics," Journal of Emerging Technologies and Innovative Research (JETIR), vol. 11, no. 4, pp.k48–k52, Apr. 2024.

- [9] Thamizharasan and V. Parthipan, "Design of Efficient Binary Multiplier Architecture Using Hybrid Compressor with FPGA Implementation," *Scientific Reports*, vol. 14, no. 8492, Apr. 2024,
- [10] Sujata S. Chiwande and P. K. Dakhole, "Ultra Efficient Reversible Logic Multiplier Design and Implementation for Low Power Application," *International Journal of Intelligent Systems and Applications in Engineering*, vol. 12, no. 10s, pp. 415–422, 2024
- [11] Rama Krishna Reddy, R. Tarun, C. A. Kumar, and M. V. Rao, "An Efficient Adiabatic 4-Bit Array Multiplier for Low Power Applications," *International Journal of Advanced Research in Innovative Ideas in Engineering*, vol. 10, no. 2, pp. 3711–3712, 2024
- [12] VamshiPonugoti, S. Poloju, S. Oruganti, and S. Bopidi, "Design of Baugh Wooley Multiplier Using Full Swing GDI Technique," *EasyChair Preprint*, no. 5374, Apr. 2021
- [13] BhargaviKasturi and Srinivasa Rao Balagani, "Effective GDI-Based Array Multiplier and Braun Multiplier with TSMC 45nm," *International Journal of Innovative Research in Technology*, vol. 7, no. 5, Oct. 2020
- [14] S. Pousia and K. Murugan, "VLSI Implementation of High Speed Low Power Design Using Hybrid Power Gating Technique," *IOP Conf. Ser.: Mater. Sci. Eng.*, vol. 1084, no. 1, p. 012058, 2021
- [15] K. Gupta, V. Gosain, and N. Pandey, "Adiabatic Differential Cascode Voltage Switch Logic (A-DCVSL) for low power applications," *J. King Saud Univ. - Eng. Sci.*, vol. 34, pp. 180-188, 2022
- [16] L. Bigelli, C. Contoli, V. Freschi, and E. Lattanzi, "Privacy preservation in sensor-based Human Activity Recognition through autoencoders for low-power IoT devices," *Internet of Things*, vol. 26, p. 101189, 2024
- [17] N. Mantravadi, S. Rooban, G. M. Shankar, M. U. Suryad, N. Saikrishna, and A. V. Prabu, "Design and Implementation of Low-Power Dynamic Comparator," *Turk. J. Comput. Math. Educ.*, vol. 12, no. 9, pp. 538-544, 2021.