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Design of a 32-bit FPGA layout based on ALU employing reversible logic gates

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Abstract - The Arithmetic Logic Unit (ALU) is crucial core part of processors, responsible for performing arithmetic and logical operations. Traditional ALUs are designed by using irreversible logic gates that leads to higher power consumption and increased delay due to the loss of information during computation. To overcome from these limitations, in the proposed 32-bit ALU model is designed based on reversible logic gates. The main objective of this model is to improve both energy efficiency and performance by reduce the input information loss. The proposed design reduces power dissipation while supporting a wide range of arithmetic and logical operations. This occupies 3% of the total memory in FPGA and saves area by 91% compared to the traditional design. The implementation shows better performance in terms of speed, area and power, this is suitable solution for low-power VLSI applications.

Keywords — Reversible Logic Gates, 32-bit ALU, Low Power Design, FPGA Implementation, Energy Efficient Computing.

1. INTRODUCTION

The Arithmetic Logic Unit (ALU) is a core component of any processor. The ALU performs both arithmetic and logical operations. The overall efficiency of a digital system largely depends on the performance of its ALU. Conventional ALUs are designed using irreversible logic gates, which leads to higher power consumption and increased delay due to the loss of information during computation. This is a problem in VLSI systems because they need low power and high speed.

To overcome these drawbacks, the reversible logic gates are used to design the ALU. Reversible logic gates such

as Peres, Feynman, Toffoli, Fredkin, and NOT gates,thatthat helps to reduce the loss of input information, which helps in reducing energy loss.

This ALU perform operations such as addition, subtraction and bit by bit multiplication along with logical functions like AND, NAND, OR, NOR, XOR, XNOR, and NOT. Therefore this ALU performs 16 operations by consuming low power and increasing the speed. This 32-bit ALU is designed using reversible logic gates by cascading 32 identical of 1-bit ALU units. This design helps in reducing power consumption and improving efficiency, making it suitable low-power digital systems.

A. Reversible Logic gates

Reversible logic gates are special types of logic gates where the input can be uniquely obtained from the output. In simple words, no input information is lost during the operation. Because of the reversible logic property, which helps in reducing energy loss and power consumption. The reversible gates are Toffoli, Peres, Feynmen, Fredkin, NOT gates. The reversible logic gates has equal number of inputs and equal number of output.The operations of the reversible logic gates are discussed below.

(a) NOT GATE

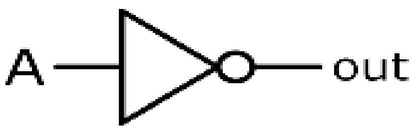

Fig1: NOT gateThe NOT gate is the simplest reversible gate and works with a single input. It simply gives the opposite value of the input. Therefore output of the not gate is the complement of the given input.

(b) FEYNMAN GATE

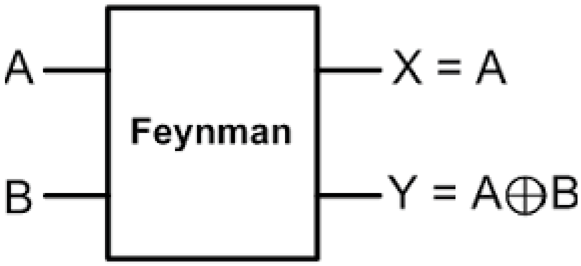

Fig2: Feynman gate

The Feynman gate is a 2×2 reversible gate, also known as the Controlled NOT gate. It has two inputs and two outputs. This gate is mainly used for copying signals. It is also useful in designing XOR-based operations.

(c) TOFFOLI GATE

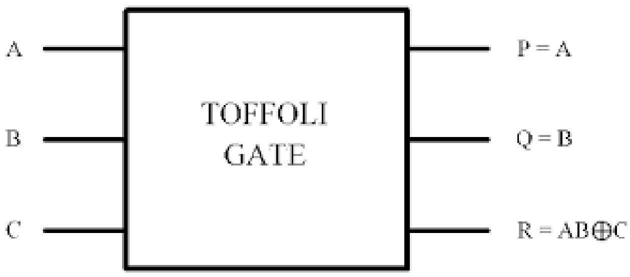

Fig3: Toffoli gate

The toffoli gate is a 3×3 reversible gate and is also known as a universal gate because it can be used to implement any logical function. And it is usually used to building complex circuits like full adders, multipliers, and control logic.

(d) PERES GATE

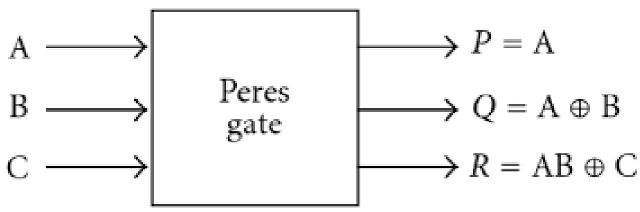

Fig4: Peres gate

The Peres gate is also a 3×3 reversible gate. It is mostly used gate because it is efficient and requires less resources compared to other reversible gates. In simple words the Peres gate can perform both XOR and AND operations together, which makes it very useful in

designing circuits like adders and ALUs. And also it can perform XOR operation in another output port.

(e) FREDKIN GATE

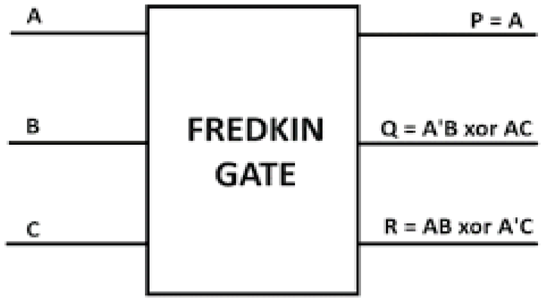

Fig4: Fredkin gate

The Fredkin gate is also a 3×3 reversible logic gate. It is also known as a controlled swap gate because it can also swap two inputs based on a control signal. When A is zero, then B and C are not swapped and when A is one the values of B and C are swapped.

2. LITERATURE SURVEY

The research papers are tried on improving the design of Arithmetic Logic Units (ALUs) to increase better speed, lower power consumption, and efficient hardware usage. In traditional ALU designs are mostly based on irreversible logic gates. These designs are simple and widely used, but power dissipation is high because of some information is lost during computation.

In several studies have shown that reversible logic gates can reduce power loss by preserving input information. That reversible gates are Feynman, Toffoli, Fredkin, and Peres are commonly used to design basic circuits like adders, subtractors and logic units. These designs are help to improve efficiency and reduce delay.

And some authors are only given the study of project. They are not implemented the project. This shows the implementation gives more knowledge than study projects.

From many previous research papers, it is observed that most of the work on reversible logic gates mainly focuses on theoretical explanation. These papers explain the concepts and working of gates, but they lack practical examples and real-time implementation. In many cases, the designs are not practically given on hardware like FPGA.

And that only allows theoretical knowledge only. This study gives that more practical work is needed for implementing the required ALU.

Some models have developed small-bit ALUs, like 4,8,16 bit designs using reversible logic. So mainly they have focused on reducing parameters like gate count, quantum cost, and garbage outputs.

The delay is also one of the main key for making the ALU. For example in previous research papers the time taken for whole operations in that ALU is also a part of designing the proposed model as speed during the computation. This shows the speed of the ALU. If speed increases then automatically the performance also improved.

In Some kind of research papers, it is observed that reversible logic helps in reducing power consumption compared to irreversible logic gates. In designs, the improvement in power is very less like in the range of 2-3 percentage. And also the area improvement is also low in terms of look up tables (LUTs).

Most of the ALU models in some research papers are designed based on the reversible gates with limited amount of operations like addition, subtractions along with logical operations .This limited amount of operations are shows the ALU efficiency with power consumption, delay.

In this paper, a 32-bit ALU is designed using reversible logic gates to overcome these limitations. The proposed design supports 16 operations.

3. PROPOSED MODEL

In Proposed model, a 32-bit Arithmetic Logic Unit (ALU) is designed using reversible logic gates to increase performance, speed and reduce power consumption. The main objective of this design is to avoid the loss of information during computation. In traditional ALU designs, some information is lost, which leads to more power consumption and heat generation for mostly large bit width. To overcome these drawbacks, reversible logic is used. Here the input information loss is reduced during computation.

The proposed ALU is designed by connecting 32 small units of 1-bit ALUs. Each 1-bit ALU performs operations on a single bit operation, and when all 32 units are cascaded, then it forms the complete 32-bit ALU. This way of design model makes the system simple, flexible. The 1-bit ALU is implemented using reversible logic gates like Feynman, Toffoli, Fredkin, Peres gates. Basic blocks are designed by using these gates like addition, subtraction, bit by by multiplication along with logical operations.

All these operations are controlled using control signals.

Based on control signals, the ALU selects and performs one operation in total operations. There are 16 operations in this model. Therefore these 16 operations are performed in proposed ALU.

The proposed model is implemented on FPGA, and it uses only about 3 percent of the total memory. And remaining more than 90 percent of memory is saved. This shows the design is very efficient in terms of memory usage of FPGA. In low memory usage, the ALU is able to perform all 16 operations properly with accurate This model is designed using the vivado 2023.1 version with Artix-7 FPGA board .

In this model, there are two inputs like A, B with 32 bit range .Here fredkin reversible gate act as a control decoder .And the output also in the range of 32 bits. And this model generates less amount of heat for mainly largr bit width.

Therefore proposed improves efficiency, reduces power consumption, increases the speed and uses hardware resources effectively with low energy loss. Due to this advantages proposed model more suitable for low-power VLSI applications and digital circuits.

(a) Block Diagram

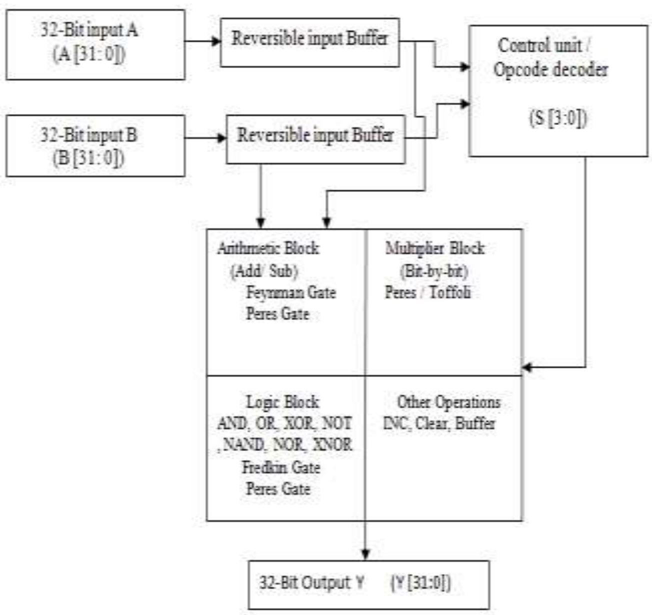

Fig5: Block diagram of proposed model

The above system takes two inputs as 32-bit input A and 32-bit input B**.** These inputs are used to perform the 16 operations. The two inputs are given to the individual reversible input buffer. This buffer makes the input data as

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no information is lost during computation. It mainly helps to maintaining the property of reversible logic.

The Control unit is opcode decoder plays an important role in the system. It helps in selection signals according to the type of operation we selected. The control unit has 4 selection lines as SEL[3:0]. That decides type of operation should be performed. So based on these control signals lines, the ALU selects the required operation.

(1) Arithmetic Block : This block performs operations like addition and subtraction by 2’s complement. This block is designed using reversible gates such as feynman and peres gates. These gates help in reducing power loss while performing arithmetic operations.

(2) Logic Block : This block used to perform the logical operations like AND, OR, XOR, NOT, NAND, NOR, XNOR. This block mainly uses Fredkin and Peres gates to perform these operations efficiently with minimal loss of input.

(3) Multiplier Block : This multiplier block used to perform the bit-by-bit multiplication. In this block, peres and toffoli gates are used to improve accurate and efficient multiplication.

(4) Other Operation Block : This block used to perform the additional operations like increment, clear, and buffer operations, which are useful for control and data handling.

The output is in the range of the 32 bits along with the carry based on given inputs for required operation.

(b) 16 Operations in ALU

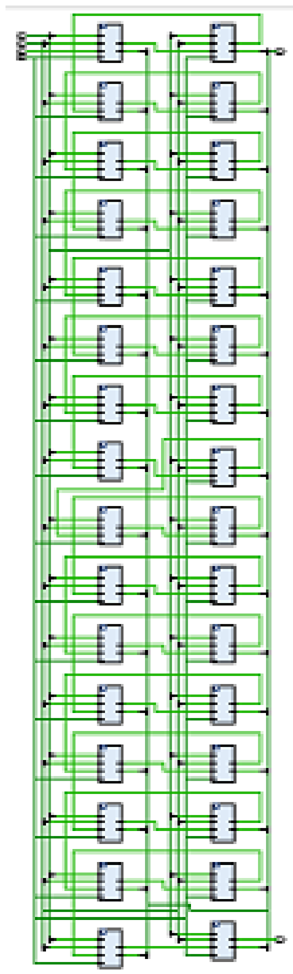
The below 16 operations are performed in the proposed 32 bit ALU model using reversible logic gates. These 16 operations are performed at a time. At every selection line, the different operation are performed.

S.NO	Output Selection line	Operation
1	0000	A + B
2	0001	A - B
3	0010	A * B
4	0011	A | B
5	0100	Complement of A
6	0101	Returns the value in R0
7	0110	XNOR
8	0111	NAND
9	1000	Clear
10	1001	NOR
11	1010	AND
12	1011	Returns value of IO status register
13	1100	Increments the value by 1
14	1101	1 * B
15	1110	XOR
16	1111	1 * A

4. RESULT ANALSIS

The proposed 32-bit reversible ALU is designed and implemented on FPGA board. The result shows the performance efficiently in terms of power, speed, and memory usage. Thus by using reversible logic gates, the system reduces input information loss. So that helps in decreasing power consumption compared to traditional ALU designs. The proposed design uses only around 3% of the FPGA memory, which shows efficiency.

(a) RTL Schematic diagram



(b) Output waveforms of 16 operations

(d) Total number of LUTs(slices)

Name	Slice LUTs (134600)	F7 Muxes (67300)	Slice (33650)	LUT as Logic (134600)	Bonded IOB (400)
ALU_REVERSIBLE_32BIT	145	32	47	145	102

(f) Comparison table of existing and proposed model

Parameters	Irreversible Gates	Reversible Gates
Power	150.3 m W	22.523 m W
Time Required to complete the all operations	320 ns	150 ns
Area(LUTs - slices)	630	145

5. CONCLUSION

In this paper, the proposed ALU model is implemented by peres, fredkin, feynman, and toffoli gates for improving overall performance. The main objective of this model is to design the ALU more efficiently in terms of power and speed. The results show that the proposed design performs better than traditional designs, especially in reducing power consumption and delay. A comparison between reversible and irreversible logic clearly shows these improvements. The design uses only about 3% of the total FPGA area, which shows that it is highly efficient. It is also observed that the delay is reduced from 320 ns to 150 ns, and the power consumption is reduced from 150.3 mW to 22.523 mW.

In the future, this paper can be expanded to build advanced digital systems using reversible logic circuits. These circuits can be applied in fields like quantum computing, low-power CMOS, nanotechnology, cryptography, optical computing, DNA computing, and other modern technologies.

6. REFERENCES

[1] P. Gopi Krishna, Penikalapati Manoj Kumar , Shaik Madeena Bibi, Mogili Venkateswararao, Sanghamu Gayatri, "Development of Comparative Design of Reversible and Irreversible 32- BIT ALUs", ISSN 2278-2540,DOI: 10.51583/IJLTEMAS, Volume XV, Issue II, February 2026.

[2] V. Sai Naveen , N. Rahim Kumar , Y. Chandra Kanth , A. Muralidhar, B. Ravi Chandra," Design And Study Of 32-Bit Arithmetic Logic Unit Block With Reversible Logic Gates ",,4 UG Scholar, 5Assoc.Professor, Department of ECE, NSRIT(A), Visakhapatnam. DOI:10.47750/pnr. 2022. 13. S09.1177.

[3] Chaithra K, Dr. K N Rajanikanth,"Performance Optimization of 32-bit alu implemented with Reversible logic using pipelining and clock gating on FPGA", International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056 Volume: 11 Issue: 11 | Nov 2024 www.irjet.net p-ISSN: 2395-0072.

[4] V. Sai Naveen , N. Rahim Kumar , Y. Chandra Kanth , A.muralidhar , B.ravi Chandra," Design And Study Of 32-bit Arithmetic Logic Unit Block With Reversible Logic Gates",Vol. 13 SPECIAL ISSUE 09 (2022).

[5] Baibaswata Mohapatra, Department Of Electrical Engineering Galgotias University, Yamuna Expressway," Review on Reversible Logic Circuits and its Application ",JETIR February 2019, Volume 6, Issue 2 www.jetir.org (ISSN-2349-5162).

[6] Li, J., & Khalid, F. FPGA Implementation of a Reversible 8-bit ALU. In Proceedings of the Internationalc onference on Field-Programmable Technology (FPT) (pp. 234-239). (2019).

[7] Tiwari, M. K., & Kumar, D. A Review on Reversible Logic Gates and Their Applications in Digital System design. IEEE Transactions on Circuits and Systems II: Express Briefs, 65(5),632-636. (2018).

[8] G. Vamsi Krishna, G. Srinivasa Rao, Y. Amar Babu," An FPGA Implementation of Low Dynamic Power & Area Optimized 32-Bit Reversible ALU ",International Journal of Applied Engineering Research ISSN 0973-4562 Volume 13, Number 5 (2018) pp. 2926-293.