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Design of Low Power TG - Based Finfet D Flip-Flop for Memory Cell Architecture

Mr. E. Satheesh Kumar , M .Tech,
Assistant Professor,
Department of Electronics and Communication Engineering,
Annamacharya Institute of Technology and Sciences, Tirupati,
esatheesh79@gmail.com

Surekha Allam ,B .Tech,
Department of Electronics and Communication Engineering,
Annamacharya Institute of Technology and Sciences,
Tirupati,
allamsurekha@gmail.com

Sravanthi Elavuru,B .Tech,
Department of Electronics and Communication Engineering,
Annamacharya Institute of Technology and Sciences,
Tirupati,
sravs7334@gmail.com

Muzahid Mandem ,B .Tech,
Department of Electronics and Communication Engineering,
Annamacharya Institute of Technology and Sciences,
Tirupati,
muzzumuzahid008@gmail.com

Sathish Kumar Koppu,B .Tech,
Department of Electronics and Communication Engineering,
Annamacharya Institute of Technology and Sciences, Tirupati,
koppusathishkumar12@gmail.com

ABSTRACT: This presents the design and analysis of a low-power transmission gate (TG)- based D flip-flop implemented using FinFET technology. The proposed architecture aims to enhance power efficiency and reduce leakage power compared to conventional CMOS-based designs. Performance evaluation is carried out by analyzing key parameters, including static power, dynamic power, and average power consumption, while ensuring reliable operation at high frequencies. Simulation results demonstrate that the TG-based FinFET D flip-flop achieves improved performance with notable power savings, making it suitable for energy-efficient memory cell applications. The proposed design exhibits a reduction in average power consumption of up to 9.36% when compared to existing designs. These results validate the effectiveness of FinFET technology for low-power, high-performance memory circuits.

KEYWORDS : FinFET technology, D flip-flop, TGFF, Memory cell,CMOS.

INTRODUCTION : The evolution of modern electronics, like high-speed processors, portable devices, and IoT applications, increases the need for compact, fast, and energy-efficient memory circuits. As technology advances to nanometer scales, CMOS transistors encounter challenges: increased leakage currents, reduced gate control, and higher power consumption. These factors reduce system performance.To fix theseproblems, FinFET technology wa introduced asan effective alternative to traditional CMOS devices. Its three-dimensional structure provides improved control over the channel. This control results in lower leakage current and better performance, especially in deeply scaled technologies [5]. These advantages make FinFETs suitable for low-power digital circuits.

In memory architectures, D Flip-Flops (DFFs) are essential components that determine the efficiency of data storage and transfer.The performance of these flip-flops directly affects key parameters, including speed, power consumption, and circuit area. Therefore, optimizing the design of DFFs is critical for achieving high-performance memory systems. In this work, a Transmission Gate (TG)-based FinFET D Flip-Flop is proposed to achieve reduced power consumption and improved operational efficiency for modern memory applications.

LITERATURE SURVEY:

The design of D flip-flops (DFFs) has been widely explored to achieve optimal trade-offs among area, speed, and power consumption in VLSI systems. With the continuous scaling of technology, power efficiency has become a critical design concern, especially for memory and sequential circuits.

In early CMOS-based DFF designs, the primary focus was on improving speed and reducing area. However, as device dimensions decreased, leakage power emerged as a significant challenge, affecting overall system efficiency [1]. To address these issues, several power reduction techniques have been proposed. Clock gating is one such approach that reduces unnecessary switching activity, thereby lowering dynamic power consumption. Despite its effectiveness, clock-gated designs introduce additional complexity and area overhead [2], [3]. Subthreshold operation has also been investigated for ultra-low-power applications, but it suffers from reduced operating speed, making it unsuitable for high-performance systems [4], [5].

Transmission gate (TG)-based DFFs have gained attention due to their ability to reduce transistor count and minimize power consumption. These designs also help in reducing signal contention and improving switching efficiency compared to conventional CMOS implementations [6], [7].

As technology continues to scale, FinFET devices have emerged as a promising alternative to planar CMOS due to their superior gate control and significantly lower leakage currents. FinFET-based designs have been shown to improve both energy efficiency and overall circuit performance, particularly in memory applications [8], [9].

Recent efforts have focused on combining transmission gate logic with FinFET technology to further enhance power efficiency. Such hybrid approaches have demonstrated substantial reductions in power consumption compared to traditional DFF architectures, with some designs reporting improvements of up to 30% [10]. In addition to power reduction, the power-delay product (PDP) is an important metric for evaluating circuit performance. Memory circuits often exhibit higher PDP due to read and write delays, making its optimization essential for achieving high-speed and low-power operation.

Furthermore, technology scaling below 48 nm introduces reliability challenges, including threshold voltage variations and increased leakage effects. FinFET devices offer improved robustness against these variations, making them suitable for advanced technology nodes. Studies on memory architectures utilizing FinFET-based DFFs indicate significant improvements in both power consumption and area efficiency compared to conventional designs.

However, achieving an optimal balance between low power consumption, high-speed operation, and reduced design complexity remains a challenge. To address this, the present work proposes a low-power transmission gate-based FinFET D flip-flop design aimed at improving energy efficiency while maintaining reliable performance for modern memory cell applications.

INTRODUCTION TO VLSI TECHNOLOGY:

The development of integrated circuit (IC) technology has significantly transformed modern electronic systems. Today's advanced devices, including computers and communication systems, rely heavily on ICs for efficient operation. The invention of the integrated circuit by **Jack Kilby** and **Robert Noyce**, which earned them the Nobel Prize in Physics in 2000, marked a major milestone in electronics.Compared to earlier designs that used discrete components, Very Large Scale Integration (VLSI) technology enables the integration of a large

number of transistors on a single chip. This results in reduced size, lower power consumption, and improved performance. As technology advances, VLSI systems allow the development of highly complex circuits with enhanced computational capability.In addition, integrated circuits offer improved reliability and simplified design compared to discrete systems. These advantages make VLSI technology essential for developing efficient and high-performance electronic systems in modern applications.

EXISTING SYSTEM:

In modern digital circuits, D Flip-Flops (DFFs) are commonly implemented using CMOS technology. These elements are widely used in memory cells, registers, and other data storage applications. However, as device dimensions shrink to the nanometer scale, CMOS-based DFFs encounter several limitations.

- Increased leakage power during standby operation
- High power consumption due to continuous clock switching
- Higher propagation delay at reduced supply voltages
- Presence of short-channel effects, which degrade performance and reliability

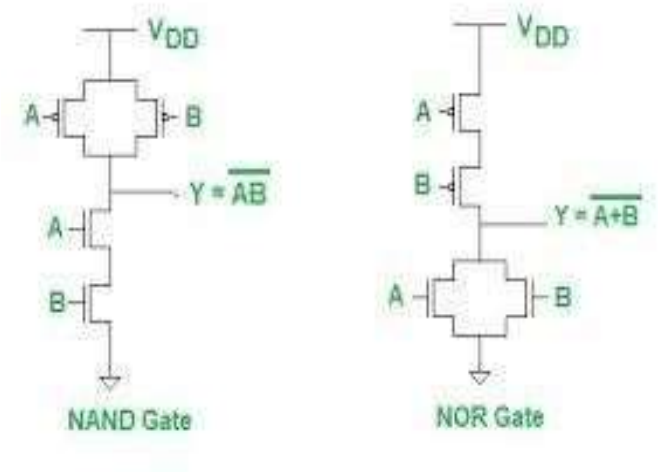


Fig (a): NAND and **NOR** using **CMOS Logic**

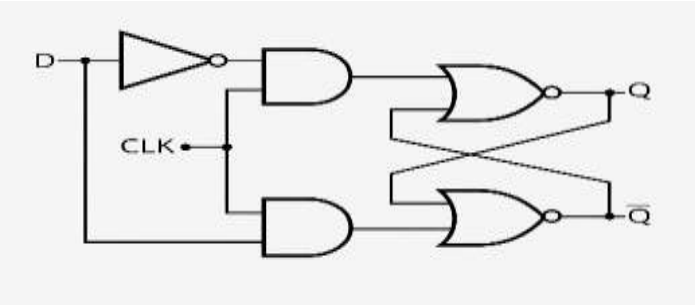
To design D Flip-Flop 22 transistors are used using cmos logic.

Due to these challenges, conventional CMOS D Flip-Flops are not well-suited for low-power and high-speed applications. Hence, there is a need for an improved design that can reduce power consumption while maintaining high performance.

ANALYSIS OF D-FLIPFLOP(EXISTING):

D Flip-Flops (DFFs) are fundamental sequential elements used in synchronous digital systems for data storage and timing control. They operate based on edge-triggering, where the input data is sampled only at the rising or falling edge of the clock signal and retained until the next clock event, ensuring stable and reliable operation.In general, a D Flip- Flop is implemented using pass transistors or transmission gates in CMOS technology. Among these, transmission gate-based designs are widely used due to their ability to provide full voltage swing and improved signal integrity. These designs offer an effective balance between power consumption, speed, and circuit area.

Structurally, a D Flip-Flop consists of two cascaded latches controlled by complementary clock signals. The first stage, known as the master latch, captures the input data, while the second stage, called the slave latch, transfers the data to the output during the clock transition. This arrangement ensures that the output changes only at the clock performance of flip-flops by reducing leakage current, improving gate control, and minimizing short-channel effects. In such implementations, each latch is formed using transmission gates and inverters built with FinFET devices. These components control the flow of data based on the clock signal, enabling efficient and low-power operation suitable for modern VLSI applications.



Fig(1) : Traditional D – Flip Flop Circuit Diagram

PROPOSED SYSTEM:

(PROPOSED D-FLIP FLOP) -D flip-flops (DFFs) are essential sequential building blocks in synchronous digital systems, playing a critical role

in data storage, timing control, and synchronization of digital signals. They are widely used in memory elements, registers, counters, and pipeline architectures. Among the different DFF architectures, transmission gate (TG)-based designs have gained significant attention due to their inherent advantages such as low power consumption, reduced propagation delay, and compact circuit implementation. By effectively minimizing redundant switching activity, especially in the clock network, TG-based DFFs help in reducing dynamic power dissipation, which is a major concern in modern low-power VLSI systems [13].

In this work, a TG-based FinFET D flip-flop utilizing High Threshold Voltage (HVT) devices is proposed to further enhance power efficiency by reducing both leakage and static power consumption. As technology continues to scale down, leakage power has become a dominant factor in overall power dissipation. Compared to Standard Threshold Voltage (SVT) and Low Threshold Voltage (LVT) devices, HVT transistors exhibit significantly lower leakage currents, thereby improving energy efficiency, particularly in nanoscale technologies. Additionally, the use of FinFET devices provides superior electrostatic control over the channel, effectively suppressing short-channel effects and improving device reliability and performance stability under scaled conditions.

The proposed DFF is designed using a master–slave configuration, which is controlled by complementary clock signals (CLK and $C\bar{L}K$) to achieve edge-triggered operation. In this configuration, the master stage samples and holds the input data during one phase of the clock, while the slave stage transfers the stored data to the output during the opposite clock phase. This arrangement ensures proper synchronization and prevents data corruption due to race conditions. Transmission gates are employed within the design to enable full voltage swing operation, thereby reducing signal degradation and improving noise margins. This leads to more reliable data transfer and better overall circuit performance.

Furthermore, TG-based DFF designs require a smaller number of transistors compared to conventional logic styles, resulting in reduced silicon area and making them highly suitable for high-density VLSI applications such as register files, shift registers, and cache memory structures [14]. To further enhance robustness, techniques such as adaptive body biasing can be incorporated to improve tolerance against process, voltage, and temperature (PVT) variations, which are critical challenges in nanoscale designs [15]. In comparison to traditional pass-transistor logic, the proposed TG- based FinFET DFF offers improved signal integrity due to its full voltage swing characteristics, as well as enhanced reliability under varying operating conditions [16].

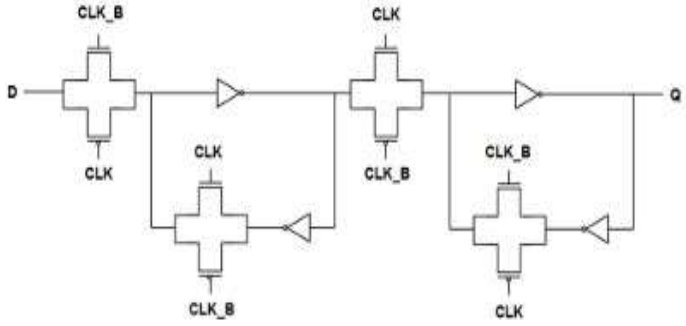


Fig 2. Transmission Gate D-Flip Flop

Figure 2 illustrates the proposed transmission gate (TG)-based FinFET D flip-flop architecture. The design is optimized to achieve reduced power consumption by minimizing both dynamic and leakage components, while also maintaining a compact circuit layout. The use of FinFET technology enhances electrostatic control and reduces short-channel effects, thereby improving overall device reliability. Additionally, the incorporation of transmission gates ensures full voltage swing operation and better signal integrity. Owing to these advantages, the proposed design offers efficient performance and is well-suited for modern low-power VLSI applications, particularly in memory and sequential circuit implementations.

ANALYSIS OF MEMORY CELL: The proposed transmission gate (TG)-based FinFET D flip-flop enhances memory cell performance while improving overall energy efficiency. In modern VLSI systems, reducing power consumption is a major design challenge, especially in battery- powered and low-energy applications where memory elements contribute significantly to total power usage. The use of FinFET technology in the proposed design provides improved gate control and effectively reduces leakage current, thereby minimizing static power dissipation.

In addition, transmission gate logic helps in lowering dynamic power consumption by reducing unnecessary switching activity and enabling efficient signal transfer. The design also ensures full voltage swing operation, which improves signal integrity and noise margins, contributing to reliable circuit performance. The optimized structure further supports compact implementation, making it suitable for high-density memory applications.

Simulation results demonstrate that the proposed memory cell achieves noticeable power savings compared to conventional CMOS-based D flip- flops. These improvements are mainly due to reduced switching transitions and the efficient combination of TG logic with FinFET devices.

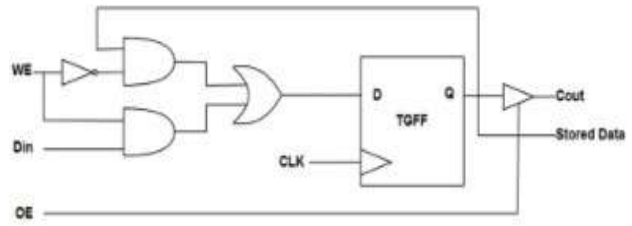


Fig 3. Memory Cell Diagram

Fig (3): illustrates the memory cell architecture, highlighting its compact and efficient design. Hence, the proposed approach is well suited for low- power applications such as smartphones and IoT devices [20]–[21].

SOFTWARE TOOL:(TANNER EDA)

Tanner EDA is used for the backend design and verification of a TG-based FinFET D flip-flop.

Initially, the schematic of the proposed and existing D flip-flops is designed using S-Edit, which allows easy construction and visualization of the circuit. The designed circuits are then analyzed using T- Spice, the simulation engine of Tanner EDA, to evaluate key performance metrics such as power consumption, propagation delay, voltage swings, and transient response. The output waveforms are observed using W-Edit, which helps verify the correct operation of the flip-flops and compare the behavior of the proposed design with the existing one.

Tanner EDA also supports backend design verification, enabling the creation of circuit layouts and execution of design rule checks and layout- versus-schematic (LVS) verification. These steps ensure that the circuit is optimized, manufacturable, and reliable. The tool allows testing under different operating conditions, such as varying supply voltages and process variations, making it possible to design energy-efficient, high-speed, and robust flip-flops.

Overall, Tanner EDA provides a complete platform for schematic design, simulation, waveform analysis, and backend verification, ensuring accurate evaluation and validation of VLSI circuits before fabrication.

- **S-Edit :** Schematic Design
- **T-Spice :** Circuit Simulation
- **W-Edit :** Waveform Analysis
- **L-Edit :** Layout Design
- **LVS :** Layout Verification

SCHEMATIC DIAGRAMS OF EXISTING AND PROPOSED SYSTEM:

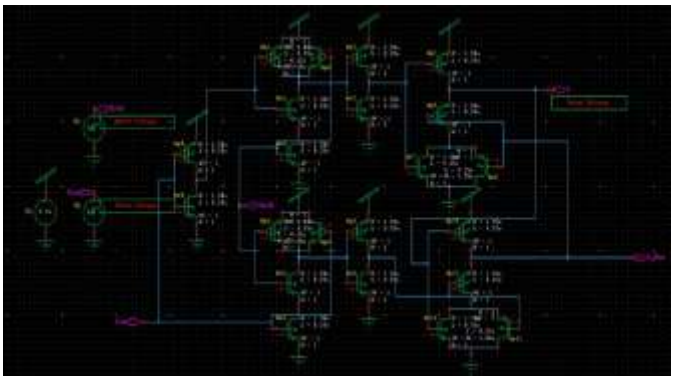


Fig (4): Existing System (Traditional D FlipFlop)

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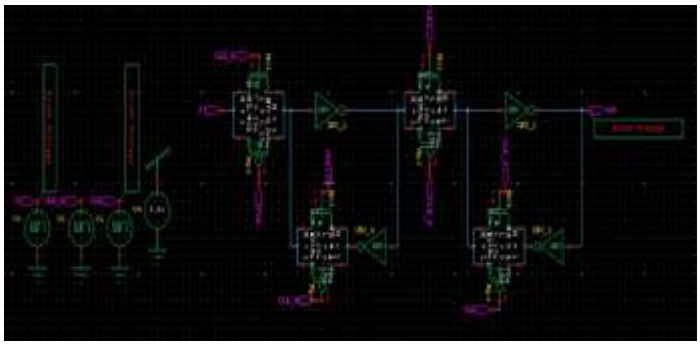
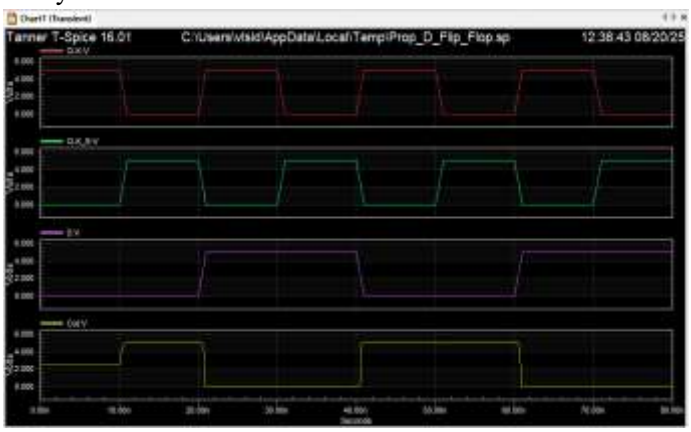


Fig(5): Proposed system (TG based D FlipFlop)

Fig(6): Memory cell architecture with proposed D FlipFlop

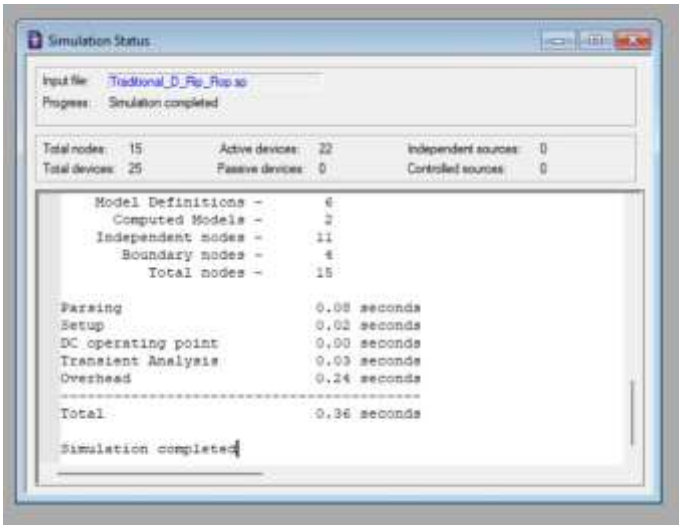
RESULTS: A D Flip-Flop stores and transfers data based on the clock signal, producing an output waveform that reflects its operation. When a clock edge occurs, the flip-flop samples the D input and updates the output Q accordingly. The output retains this value until the next relevant clock edge, ensuring that changes at the input between clock transitions do not affect the stored value. This behavior makes the D Flip-Flop a key element in sequential logic circuits, as it provides stable and synchronized data for subsequent stages, preventing unwanted transitions and maintaining proper timing within the system.



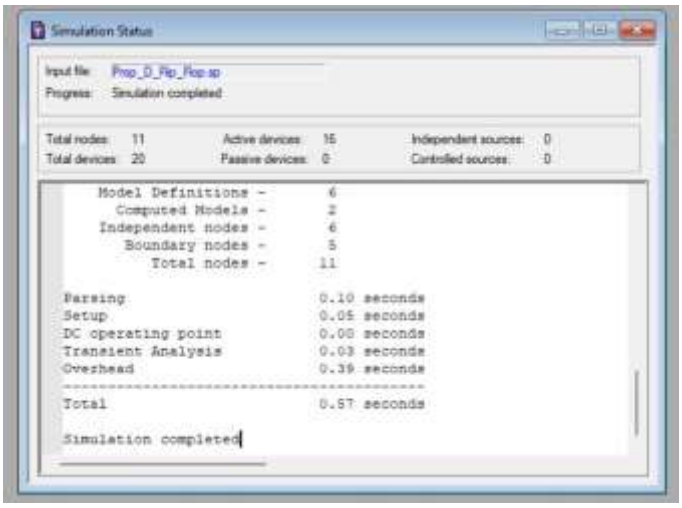
Fig(7): Output Waveform

The above waveform shows that the output of the D Flipflop for given input and clock signals.

SIMULATION OUTPUT :



Fig(8): Traditional D Flipflop



Fig(9): Proposed D FlipFlop

CONCLUSION:

Thus,we propose a low-power FinFET D flip-flop based on a transmission gate (TG), designed for memory cell applications. By combining the efficient TG configuration with the advantages of FinFET technology—such as reduced leakage current and improved gate control—the design achieves significant power reduction without sacrificing performance. Compared to conventional D flip-flops, the proposed design demonstrates lower average and leakage power, making it well- suited for low power memory architectures. Comprehensive simulations and analyses indicate that this TG-based FinFET D flip-flop provides a strong power-performance trade-off and is promising for integration into modern memory cells. This approach addresses critical challenges in

power-sensitive applications, including portable electronics and IoT devices, and contributes to the development of low-power digital circuits in scaled technologies.

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REFERENCES:

[1] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," IEEE J. Solid-State Circuits, vol. 24, no. 1, pp. 62-70, 1989.

[2] W. Zhao et al., "Low power flip-flop design with reduced clock load," IEEE Trans. Circuits Syst., vol. 53, no. 6, pp. 1190-1198, 2006.

[3] P. M. Lee et al., "A low power flip-flop design for high-performance applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 5,
pp. 850-854, 2011.

[4] L. Wang and N. Wang, "Design of low power high-performance flip flops," IEEE Trans. Circuits Syst., vol. 67, no. 2, pp. 340-350, 2020.

[5] N. Verma and A. P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense- amplifier redundancy," IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 141-149, 2008.

[6] M. Keating and D. Flynn, "Low Power Methodology Manual: For System-on-Chip Design," Springer, 2007.

[7] B. Nikolic et al., "A 1.06 GHz 16 × 16 b multiplier in 0.18 μm CMOS," IEEE J. Solid-State Circuits, vol. 37, no. 2, pp. 1190-1198, 2002.

[8] T. Kuroda et al., "Low-power CMOS digital design," IEEE Micro, vol. 19, no. 2, pp. 8-18, 1999.

[9] X. Sun et al., "Design optimization of FinFET based circuits," IEEE Trans. Electron Devices, vol. 60, no. 1, pp. 152-162, 2013.

[10] M. Khellah et al., "Low power circuits and technology in VLSI," IEEE Trans. VLSI Syst., vol. 15, no. 4, pp. 1-10, 2007.

[11] K. Roy et al., "Leakage current mechanisms and leakage reduction techniques in deep-submicron CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305- 327, 2003.

[12] J. P. Duarte et al., "FinFET process technology: Challenges and opportunities," IEEE Trans. Electron Devices, vol. 57, no. 1, pp. 89-98, 2010.

[13] A. Sahoo, A. Pattanaik, and S. S. Mahapatra, "Low-power transmission gate-based D flip-flop for portable applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 8, pp. 1621-1625, 2014.

[14] K. Shah, P. Kumar, and S. Yadav, "Area- efficient D flip-flop design using transmission gate logic," IEEE International Conference on VLSI Design and Embedded Systems, pp. 334-338, 2015.

[15] C. Lee, H. Song, and S. Kim, "A robust transmission gate-based flip flop tolerant to PVT variations," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 10, pp. 2878- 2886, 2014.

[16] M. Alioto and G. Palumbo, "Noise margin and robustness analysis of transmission gate flip-flops," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 1, pp. 156-167, 2010.

[17] Taghipour, Shiva, and Rahebeh Niaraki Asli. "Aging comparative analysis of high-performance FinFET and CMOS flip-flops." Microelectronics Reliability 69 (2017): 52-59.

[18] Absel, Kalarikkal, Lijo Manuel, and R. K. Kavitha. "Low-power dual dynamic node pulsed hybrid flip-flop featuring efficient embedded logic." IEEE transactions on very large-scale integration (vlsi) systems 21.9 (2012): 1693-1704.

[19] Lanuzza, Marco, et al. "Comparative analysis of yield optimized pulsed flip-flops." Microelectronics Reliability 52.8 (2012): 1679-
1689.

[20] Dhanasekar, S. "An area efficient vedic multiplier for FFT processor implementation using 4-2 compressor adder." International Journal of Electronics 111.6 (2024): 935-951.

[21] Govindaraj, V., et al. "Minimum power test pattern generator for testing VLSI circuits." 2022

6th international conference on devices, circuits and systems (ICDCS). IEEE, 2022.

[22] Arunkumar, N., et al. "An ultra-low-power static random-access memory cell using tunneling field effect transistors." International Journal of Engineering 33.11 (2020): 2215-2221.

[23] Dhanasekar, S., and V. Govindaraj. "Low- power test pattern generator using modified LFSR." Aerospace systems 10 (2023).

[24] Dhanasekar, S., P. Malin Bruntha, and K. Martin Sagayam. "An improved area efficient 16- QAM transceiver design using Vedic multiplier for wireless applications." International Journal of Recent Technology and Engineering 8.3 (2019): 4419-4425.

[25] Dhanasekar, S., et al. "An area efficient FFT processor using modified compressor adder based Vedic multiplier." 2022 6th International Conference on Devices, Circuits andSystems (ICDCS). IEEE, 2022.