International Scientific Journal of Engineering and Management (ISJEM) ISSN: 2583-6129
Volume: 04 Issue: 07 | July – 2025 DOI: 10.55041/ISJEM04753
An International Scholarly || Multidisciplinary || Open Access || Indexing in all major Database & Metadata

Design of MIPI CSI-2 Protocol at IP Level

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***Abstract*—The integration of high-resolution imaging in modern medical diagnostic devices demands a robust, efficient, and standardized data interface between image sensors and processing units. The Mobile Industry Processor Interface (MIPI) Camera Serial Interface 2 (CSI-2) protocol, originally developed for mobile and embedded applications, is increasingly being adopted in medical imaging systems due to its high-speed, low-power, and scalable communication capabilities. This work presents the design and implementation of the MIPI CSI-2 protocol tailored for medical imaging applications, focusing on reliable transmission of real-time image data from high-resolution sensors to processing units. The proposed design covers the protocol's layered architecture, including packet formatting, virtual channel utilization, error handling, and flow control mechanisms. Implemented using System Verilog, the design is verified using simulation and synthesis tools, ensuring accurate data transmission over the MIPI D-PHY physical layer. Emphasis is placed on low latency, deterministic performance, and minimal power consumption - critical factors in medical environments where precision and reliability are paramount. The CSI-2 protocol's flexibility enables integration into various medical imaging modalities, enhancing data fidelity and system responsiveness. This work lays the groundwork for the adoption of standardized, high-efficiency interfaces in next-generation medical imaging devices.**

Keywords— MIPI CSI-2, Medical Imaging, D-PHY, Real-Time Image Transmission, Low Power Interface, High-Speed Data Transfers.

I. INTRODUCTION

The MIPI CSI-2 (Camera Serial Interface-2) protocol is a high-speed, energy-efficient interface standardized by the MIPI Alliance to enable seamless image data transmission between camera modules and processors in embedded systems. As imaging requirements in modern electronic devices continue to grow—demanding higher resolutions, faster frame rates, and low power consumption—CSI-2 has become the de facto standard across a wide spectrum of applications. Designed with scalability and flexibility in mind, CSI-2 supports data rates up to 8 Gbps per lane, accommodating single and multi-lane configurations. This makes it highly suitable for high-resolution image capture and real-time video streaming. Furthermore, its ability to support multiple image formats including RAW, YUV, RGB, and JPEG allows it to cater to a broad range of imaging systems, from consumer electronics to specialized industrial and medical equipment. At the physical layer, CSI-2 leverages differential signalling technologies such as D-PHY and C-PHY, which offer low electromagnetic interference (EMI), high signal integrity, and minimal power consumption. These physical layers are critical for maintaining robustness in noisy environments and ensuring consistent, synchronized transmission over small and large distances. Data is encapsulated and transmitted in well-defined packets, governed by the CSI-2 protocol's layered architecture. This packetized transmission enables efficient control, error handling, and synchronization, essential for maintaining the accuracy and reliability of image data transfer. Due to its compact footprint, low power profile, and high throughput, MIPI CSI-2 is now integral to numerous imaging applications, including smartphones, automotive systems (ADAS), medical imaging devices, augmented and virtual reality (AR/VR), and IoT-enabled smart cameras. This project focuses on the design and implementation of the CSI-2 protocol at the IP level, making it suitable for integration into System-on-Chip (SoC) architectures. The objective is to create a modular, reusable IP core that adheres to MIPI specifications, ensures protocol compliance, supports high data integrity, and interfaces efficiently with both the sensor and processor subsystems. By targeting IP-level design, the work enables faster prototyping, easier customization, and optimized performance for advanced embedded imaging applications.

II. LITERATURE REVIEW

The MIPI CSI-2 protocol has become a widely adopted standard for image data transmission in embedded vision systems, owing to its ability to deliver high-speed, low-power, and low-latency communication between image sensors and processing units. Introduced by the MIPI Alliance, the protocol plays a crucial role in enabling compact and efficient camera interfaces for various high-resolution and real-time imaging applications. The CSI-2 specifications, as documented in official releases [1][2][5], define a layered protocol architecture that facilitates packet-based data transfer. These layers ensure effective encapsulation, error detection, and transport of image streams across the interface. The physical transmission is handled through differential signalling standards—D-PHY and C-PHY—which significantly reduce electromagnetic interference (EMI) while maintaining signal integrity and synchronization, especially at high data rates of up to 8 Gbps per lane.

The robustness and adaptability of CSI-2 have been validated through multiple research efforts. In a notable study by F. Liu, L. Wang, and Y. Yang [3], a UHD (Ultra-High Definition) image acquisition system using CSI-2 was implemented on an FPGA platform. Their research highlights the protocol's capability to support scalable resolutions and real-time data handling, key requirements in video processing

and surveillance applications. Moreover, their work brings attention to several implementation-level challenges, such as resource optimization, data throughput balancing, and protocol compliance in reconfigurable hardware environments. Another critical component in CSI-2 system design is the physical layer interface, especially the D-PHY standard (v1.2) [4]. This layer governs voltage levels, timing parameters, lane alignment, and signal skew control, which are essential for seamless integration of the protocol into high-speed SoC designs. Any inaccuracies at this level can result in synchronization errors, data corruption, or link failure, emphasizing the importance of strict adherence to the specification during IP-level implementation. Together, these studies and technical documents provide a strong foundation for understanding the theoretical and practical aspects of CSI-2. They emphasize the need to carefully address latency, bandwidth utilization, packet synchronization, and power efficiency all of which are critical when designing an IP-level implementation that interfaces directly with camera modules and processing subsystems in an SoC environment. This project builds on the insights from these works to realize a modular, standards-compliant IP core for CSI-2, focusing on reusability, hardware optimization, and seamless integration with imaging pipelines in embedded systems...

III. Overall System Design

1. Proposed Method

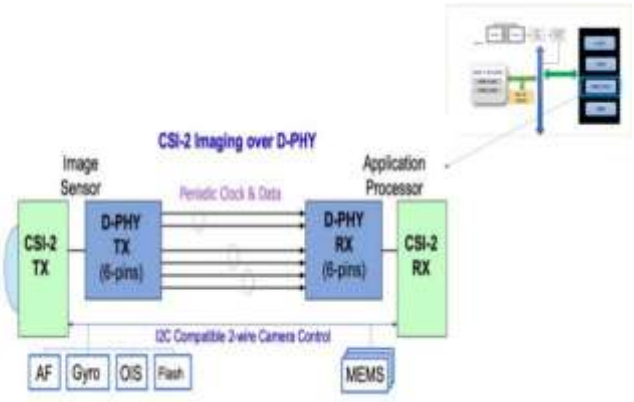
The proposed design focuses on the IP-level implementation of the MIPI CSI-2 protocol, enabling efficient image data transfer between camera sensors and application processors in embedded systems. The architecture is structured to maintain protocol compliance, ensure high-speed communication, and optimize system integration within a SoC (System-on-Chip) platform.

1.1 Proposed Block Diagram of MIPI CSI-2

The objective of this project is to design and implement the MIPI CSI-2 protocol at the IP level, enabling seamless and high-speed transmission of image data from camera sensors to embedded processors. The approach focuses on creating a reusable and configurable hardware IP that can be integrated into custom SoCs (System-on-Chip) for real-time imaging applications. The proposed method leverages the layered structure of the MIPI CSI-2 protocol, starting from the Camera Sensor Interface (CSI-2 TX) block on the sensor side, followed by D-PHY TX for high-speed serial transmission, and ending with D-PHY RX and CSI-2 RX on the processor side. The goal is to implement the CSI-2 receiver IP core that is compliant with the MIPI specifications and integrates tightly with the processor subsystem. The MIPI CSI-2 IP core is embedded within an SoC platform based on the RISC-V RV32ISC processor architecture, also shown in Fig1. This processor acts as the control unit, managing the image data flow, memory access, and configuration of camera control interfaces. The system also includes peripherals such as SRAM (128KB) for temporary image buffering and external memory interfaces like DDR, UART, and QSPI. The CSI-2 IP is memory-mapped and bus-connected via a standard on-chip bus interface, allowing smooth communication with the CPU and other peripherals.

Fig.1. Block diagram showing MIPI CSI-2 over D-PHY communication and integration with SoC configuration.

As shown in Figure 1, image data generated by the sensor is first packetized using the CSI-2 protocol. This data is



transmitted across differential serial lanes using the D-PHY physical layer, which supports multiple data lanes (typically 4 data lanes and 1 clock lane) to allow high bandwidth and low EMI communication. The receiver side D-PHY decodes the differential signals and passes them to the CSI-2 RX IP, which interprets packet headers, performs line and frame synchronization, and outputs pixel data in a parallel format. From the master configuration side, this design enables programmable control of CSI-2 parameters, such as lane number, data type filtering, and error detection logic.

This flexibility ensures compatibility with a wide range of camera modules and allows adaptation to different resolution and frame rate requirements. This method not only ensures compliance with MIPI CSI-2 standards but also provides a lightweight, power-efficient, and scalable IP block, suitable for embedded platforms used in medical imaging, ADAS, IoT cameras, and AR/VR systems. The modularity of the IP allows it to be reused across projects, facilitating rapid prototyping and time-to-market efficiency in imaging SoC designs.

1.2 Comparison of bus efficiency between USB: MIPI CSI-2

This work presents a custom MIPI CSI-2 Receiver IP core, designed for integration within a RISC-V-based SoC to enable high-speed image data reception from camera modules. The IP core operates alongside a D-PHY interface, receiving serialized pixel packets, decoding protocol headers, performing CRC/ECC checks, and outputting synchronized parallel image data. The receiver is fully configurable via software-accessible registers from the master processor side, allowing dynamic control over lane usage, virtual channel selection, and error monitoring. This approach ensures flexibility, protocol compliance, and system-level adaptability for various imaging needs.

Compared to traditional interfaces like USB, CSI-2 offers significantly lower transmission overhead and higher efficiency, as illustrated in Fig 2. CSI-2 utilizes dedicated lanes for data and clock through D-PHY, delivering superior

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throughput for embedded applications such as medical imaging, ADAS, and IoT vision systems.This IP-level implementation ensures reusability, scalability, and low power consumption, making it ideal for SoC designs requiring real-time, high-bandwidth image acquisition.

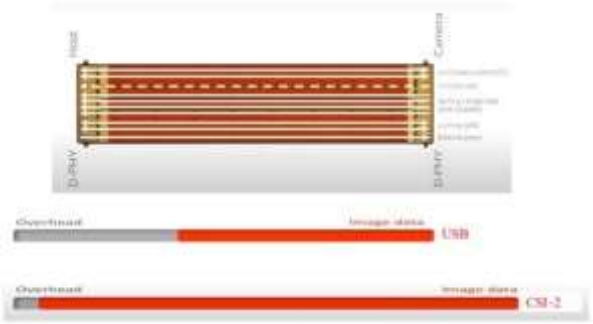

Fig. 2. Bus efficiency comparison of USB vs. MIPI CSI-2, highlighting CSI-2 higher data throughput and lower protocol overhead.

1.3 *Dynamic lane selection and byte-wise data alignment in CSI-2 receiver*

This work proposes the development of a configurable MIPI CSI-2 Receiver IP core for efficient, low-latency image data transfer in embedded systems. The IP is designed to decode packetized data streams transmitted over D-PHY lanes from an image sensor to an SoC platform. The CSI-2 RX core interfaces with the physical layer and extracts pixel data by identifying data types, decoding headers, and aligning bytes in accordance with the byte clock, as shown in Fig. 3. The design supports up to four data lanes, with active lane selection logic to adaptively align and unpack incoming bytes into parallel outputs. The use of packed data alongside a synchronized byte clock ensures high throughput and protocol timing compliance. Configuration is done via master-side software registers (RISC-V based), allowing control over virtual channel mapping, error detection, and frame synchronization. Compared to generic data interfaces, CSI-2 significantly reduces protocol overhead and improves data efficiency, making it ideal for applications like real-time imaging, ADAS, and wearable vision systems.

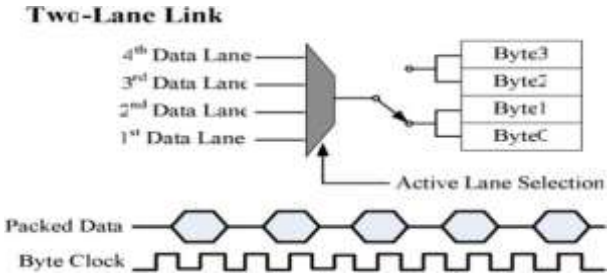

Fig.3. Dynamic lane selection and byte-wise data alignment in CSI-2 receiver using byte clock.

1.4 Frame Format MIPI CSI-2

This work presents a configurable CSI-2 Receiver IP core designed to decode MIPI packet-based image data over D-PHY lanes. The IP core processes both short and long packets, handling key protocol elements such as Start of Transmission (SoT), Packet Header (PH), Data, Packet Footer (PF), and End of Transmission (EoT). It accurately extracts image frames marked by Frame Start (FS) and Frame End (FE) signals, as shown in Fig. 4, and synchronizes data using VVALID, HVALID, and DVALID control signals. Low-power states between image lines are efficiently managed using LPS signalling, while the receiver supports proper byte alignment and error detection. Configuration is achieved through memory-mapped registers controlled by a master RISC-V processor, enabling runtime flexibility over lane count, error flags, and channel selection.

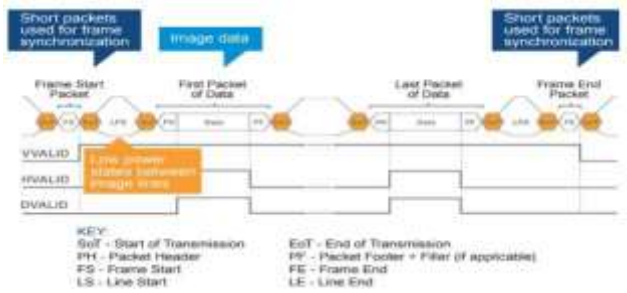

Fig.4. CSI-2 packet structure with synchronization

The proposed method ensures full protocol compliance, optimized data extraction, and seamless integration into SoC environments for real-time, high-resolution imaging applications.

IV. Simulation Results

To validate the functionality of the MIPI CSI-2 IP core, simulation was performed using a testbench configured to mimic real-time camera input. The waveforms illustrate correct decoding of protocol signals, lane alignment, and successful image data reconstruction at the receiver end.

A. Simulation waveform for CSI-2 camera module

The simulation verifies the functional behavior of the designed MIPI CSI-2 IP core. As shown in Fig. 5, the testbench drives inputs including the differential clock (clock_p, clock_n) and data lanes (data_p, data_n) to emulate real-time image sensor output. The simulation output shows correct detection of virtual_channel, image_data_type, and word_count, followed by the activation of image_data_enable.

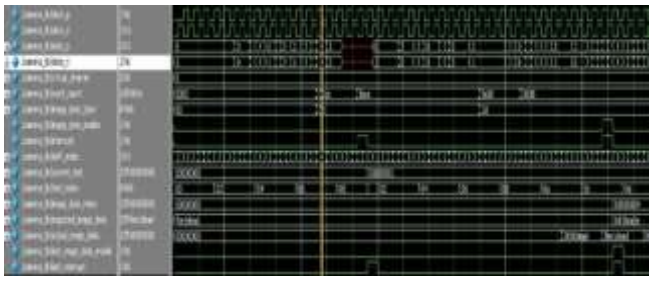

Fig.5. CSI-2 Simulation Showing Channel Detection

The correct transition of expected_image_data and actual_image_data confirms successful byte alignment and packet decoding, validating the implemented lane distribution and unpacking logic. Additionally, the interrupt and

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shift_index signals indicate proper frame boundary recognition and error handling. These results confirm the IP core's compliance with the CSI-2 protocol and readiness for integration in System-on-Chip (SoC) environments.

B. D-PHY Receiver Verification

The D-PHY module plays a critical role in facilitating robust data transmission for the CSI-2 protocol. In this design, the receiver block was implemented and verified for correct operation using simulation waveforms. As illustrated in Fig.6, the testbench provides differential clock (clock_p, clock_n) and data (data_p, data_n) inputs to simulate real sensor input. The internal shift_out and shift_in signals represent the parallel deserialization logic converting serial input data into bite-aligned values. The data and enable outputs confirm the successful decoding of valid packets in sync with the byte clock domain.

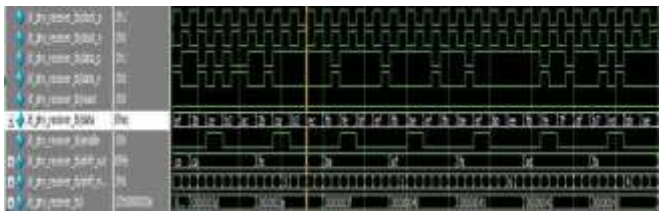

Fig. 6. D-PHY Receiver Simulation Showing Byte Alignment

The simulation confirms that data bytes were accurately sampled, shifted, and captured, demonstrating functional correctness of the physical layer interface. This validates the D-PHY module's ability to reliably receive serialized data with proper synchronization and bit-to-byte alignment essential for upstream CSI-2-layer decoding and image reconstruction.

C. Schematic View Of Camera Module

The post-synthesis simulation of the top-level integration confirms the successful functional behavior of the MIPI CSI-2 IP module. As shown in Fig. 7, the testbench drives the CSI-2 camera module through appropriate D-PHY signals (clock_p, clock_n, data_p, data_n) into the image receiver.

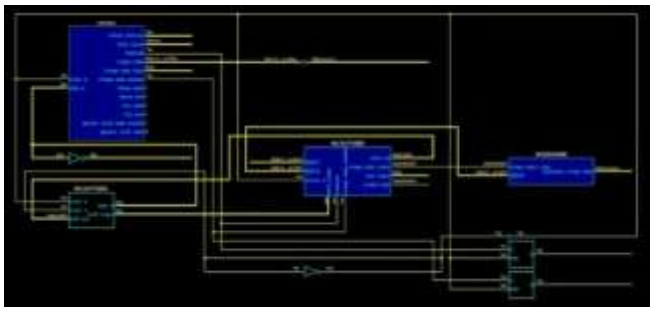

Fig.7. Schematic view of camera module

The output signals like virtual_channel, image_data, interrupt, and control flags (frame_start, line_start, generic_short_data_enable) are decoded and propagated into subsequent processing blocks. Functional blocks such as shift registers and test vectors validate the correctness of image data flow and integrity with expected values. The simulation ensures accurate synchronization, channel alignment, and protocol decoding across all modules, confirming proper IP-level behavior of the CSI-2 protocol.

D. Schematic View Of D-PHY module

The successful simulation of the MIPI CSI-2 protocol at the IP level confirms the accurate functionality of both D-PHY and camera modules. The testbench waveform demonstrates synchronized transmission of high-speed data, along with correct alignment, unpacking, and verification across virtual channels. The D-PHY receiver is responsible for deserializing the incoming data and ensuring byte alignment before forwarding it to the CSI-2 layer

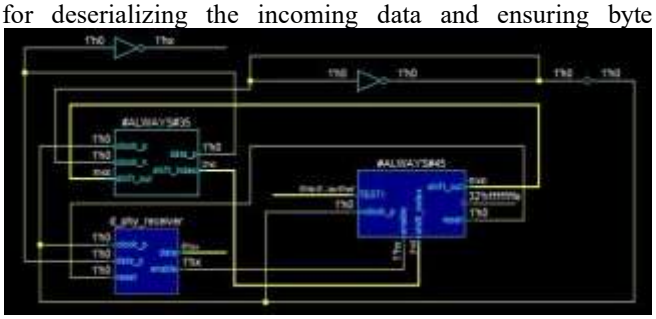

Fig.8.Schematic View Of D-PHY module

The schematic in Fig. 8 showcases the interconnection of the D-PHY receiver with surrounding logic blocks. It confirms that the design correctly handles differential clock and data inputs, aligns the serial stream using the byte clock, and forwards aligned data through the IP interface. Reset, enable, and shift logic were also validated through simulation for proper control signal management.

V. CONCLUSION

This work presents a reliable and efficient IP-level implementation of the MIPI CSI-2 protocol, optimized for high-speed medical imaging applications. The design ensures accurate data transmission with low power and latency by integrating packet formatting, virtual channels, and error handling. Verified through System Verilog simulations, it supports seamless interfacing with MIPI D-PHY and various image formats. Its modular and scalable architecture makes it well-suited for integration into next-generation medical diagnostic systems requiring precision and performance.

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