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Enhanced Self-Test and Fault Localization in VLSI Circuit Using a 32-bit LFSR

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Abstract – An Enhanced Self-Test and Fault Localization System (STFLS) improves fault detection accuracy in digital circuits. A 32-bit LFSR-based Pseudo-Random Pattern Generator generated test patterns, establishing a fault-free reference for precise comparison. Faults were identified by detecting deviations from the stored baseline outputs to ensure accurate localization. The system was implemented in Verilog HDL and simulated using Xilinx Vivado, thereby enhancing traditional self-test techniques. This approach is highly effective for VLSI testing, hardware verification, and fault analysis, and ensures improved system reliability and performance in complex digital architectures.

***Key Words*:** Fault Localization, LFSR, VLSI Testing Hardware Verification, FPGA Implementation

1. INTRODUCTION

Fault detection and localization are critical in modern VLSI systems to ensure reliability, performance, and fault tolerance in complex digital architectures. In safety-critical and high-performance applications, undetected faults can lead to system failure, increased downtime, and degraded operational efficiency. A robust testing mechanism is essential for enhancing the fault coverage, optimizing the fault isolation, and improving the circuit validation. This project presents the design and implementation of an enhanced self-test and fault-localization system (STFLS), which integrates structured test methodologies to achieve precise fault detection and localization in digital circuits.

The system employs a 32-bit Pseudo-Random Number Generator (PRNG) based on a Linear Feedback Shift Register (LFSR) to generate test patterns that systematically evaluate the circuit integrity. These patterns undergo bitwise comparison and logic analysis, establishing a fault-free reference to detect deviations in real-time outputs. Unlike conventional self-test methods, which often indicate faults at a macro level, STFLS isolates faults at a granular level, allowing targeted fault identification rather than marking the entire circuit as defective. This refined approach minimizes error propagation, enhances diagnostic precision, and facilitates efficient fault mitigation strategies in VLSI design and testing. To ensure accuracy, the system integrates cycle-wise fault detection mechanisms, storing the expected fault-free outputs and comparing them with real-time responses from the Circuit Under Test (CUT). When a mismatch is detected in specific test cycles, the system accurately pinpoints the faulty logic block, thereby reducing false positives and unnecessary circuit replacements. Additionally, a controlled fault-injection mechanism was incorporated to assess system robustness by simulating real-world defect scenarios, thereby improving the overall test reliability.

The STFLS was implemented in Verilog HDL and validated using Xilinx Vivado, ensuring seamless integration into hardware testing workflows. This methodology enhances the traditional Built-In Self-Test (BIST) approaches by offering real-time fault detection, precise fault localization, and optimized diagnostic capabilities. This system is particularly beneficial for VLSI testing, structural verification, and semiconductor reliability analysis, ensuring high test coverage and scalability. Furthermore, its adaptable design allows its deployment in Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs), making it a highly efficient solution for advanced digital circuit testing and verification.

Field-Programmable Gate Arrays (FPGAs) play a crucial role in implementing and validating fault detection and

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localization techniques owing to their reconfigurability, high-speed parallel processing, and hardware-level debugging capabilities. It is a reconfigurable block that allow users to create the design function and modify it as required.

2. SELF-TEST ARCHIETECTURE

The Self-Test Architecture consists of three key blocks: the Test Pattern Generator (TPG), Circuit Under Test (CUT), and Logic Block. These components work together to ensure efficient fault detection and localization in digital circuits, thereby enhancing the system reliability and diagnostic accuracy.

A Test Pattern Generator (TPG) plays a crucial role in generating structured stimulus signals for fault detection. In this architecture, a 32-bit Linear Feedback Shift Register (LFSR) is utilized as the TPG to produce pseudorandom test patterns. These dynamically generated test vectors served as input stimuli to the CUT, ensuring a diverse range of patterns for comprehensive fault coverage. LFSR-based pattern generation enhances the randomness while maintaining a deterministic structure, making it suitable for efficient fault detection in VLSI circuits.

The Circuit Under Test (CUT) in this architecture is an XOR tree designed to perform bitwise XOR operations on the test patterns received from the TPG. The output of the CUT was then validated against a set of precomputed golden reference values, ensuring that any deviations from the expected results could be detected. By comparing real-time CUT outputs with fault-free golden CUT values, this process ensures high-precision fault identification and classification.

The Logic Block is responsible for storing the golden CUT values and performing comparative fault analysis. It includes a comparator module that systematically evaluates the CUT output against stored reference values. If a mismatch occurs, it indicates a fault in the circuit, enabling precise fault localization. This systematic approach enhances the diagnostic accuracy, allowing for error isolation and correction.

The proposed Enhanced Fault Detection and Localization System introduces a high-precision diagnostic framework that surpasses conventional fault detection methodologies by isolating and identifying specific faulty components within the circuit rather than flagging the entire system as defective. By leveraging advanced fault analysis algorithms, this approach enhances the diagnostic accuracy and significantly reduces false positives while distinguishing between minor deviations and critical failures. By optimizing fault isolation, the model ensures efficient resource utilization, prevents unnecessary circuit replacements, and minimizes the maintenance overhead. Designed for scalability, the system seamlessly extends to complex digital architectures, thereby enabling real-time fault tracking in large-scale hardware implementations. Its robust performance and reliability make it highly suitable for digital circuit validation, processor reliability assessment, and embedded system debugging, thereby ensuring enhanced system integrity and operational resilience in high-performance VLSI applications

The figure below shows the flow diagram of the architecture.

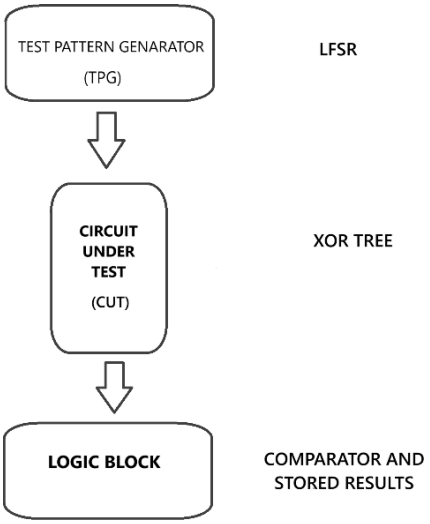

Figure 1: Flow diagram of Self-Test System

A Self-Test and Fault Localization System (STFLS) significantly enhances the reliability, robustness, and fault tolerance of digital circuits by incorporating a structured test pattern generation mechanism. This approach ensures high fault coverage, minimizes the occurrence of undetected errors, and improves the overall system integrity. By leveraging an LFSR-based Pseudo-Random Pattern Generator, the system efficiently stimulates the Circuit Under Test (CUT) with diverse input conditions, enabling comprehensive fault detection. Furthermore, this self-test methodology eliminates the dependency on external Automated Test Equipment (ATE), making it highly suitable for on-chip testing in real-time VLSI applications, including mission-critical and high-performance computing systems.

3. LFSR-BASED TEST PATTERN GENERATION

A Linear Feedback Shift Register (LFSR) is a sequential shift register that generates a deterministic sequence of pseudo-random binary values based on the feedback logic. The feedback function is defined using a characteristic polynomial that determines the sequence length before repetition. LFSRs are extensively used in Built-In Self-Test (BIST) architectures, Cryptographic applications and digital communication protocols due to their minimal hardware complexity, high-speed operation, and efficient generation of test patterns.

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The table below provides detailed information on the tap positions of 8-bit, 16-bit, and 32-bit LFSRs.

No.of bits in LFSR	Bit positions for XNOR tap points
3	3,2
4	4,3
5	5,3
6	6,5
7	7,6
8	8,6,5,4
9	9,5
10	10,7
16	16,15,13,4
32	32,22,12,1
64	64,63,61,60
128	128,126,101,99

Figure 2: Tap positions table

In the proposed Self-Test and Fault Localization System (STFLS), a 32-bit LFSR was employed as the Test Pattern Generator (TPG). The 32-bit LFSR bit length ensures a sufficiently large state space, generating nearly 4 billion unique test patterns before repetition and ensuring high fault coverage in VLSI circuits. The LFSR structure comprises 32 D-type flip-flops (FFs) connected in series, where each flip-flop stores a single bit of the sequence. These flip-flops operate as shift registers and propagate data sequentially, whereas the feedback function modifies the least significant bit (LSB) using a set of predefined tap positions.

The below figure shows the block diagram of 32-bit LFSR.

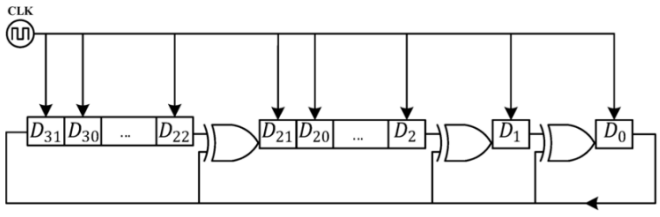

Figure 3: Block diagram of 32-bit LFSR

The 32-bit LFSR-based Test Pattern Generator efficiently produces pseudo-random test patterns for fault detection in digital circuits. This ensures high fault coverage, minimal hardware overhead, and fast operation, making it ideal for VLSI testing. The generated values are pseudo-random, meaning that they appear random but are deterministically generated based on the initial seed and feedback logic. This property allows reproducibility while maintaining randomness, enhancing reliability in self-test methodologies.

It generates a maximum of 4,294,967,295 states, as the-zero state is invalid in a typical LFSR Implementation. The shift register architecture enables efficient sequential test pattern propagation and reduces hardware complexity compared with conventional counter-based pattern generators. The tap positions define the feedback mechanism and are selected based on primitive polynomials (maximal-length polynomials) to ensure maximum randomness and a uniform distribution of patterns.

The maximal-length polynomial (max-pol) defines the tap positions in an LFSR, which determine the feedback shift operation. These tap positions ensure that the LFSR cycles through all possible 2n−1 states before repeating, thereby maximizing the randomness and distribution of the test patterns. The selection of an appropriate max-pol is crucial for achieving uniform bit transitions, enhancing fault coverage in BIST applications, and optimizing pseudo-random sequence generation for VLSI testing, cryptographic protocols, and communication systems. The flip-flops in the LFSR serve as sequential storage elements that hold each bit of the generated sequence. The shift register mechanism allows for the computation of new values based on feedback logic, thereby ensuring efficient linear test pattern generation for fault detection and diagnosis. The effectiveness of an LFSR is determined by its primitive characteristic polynomial, which determines the sequence length before repetition.

These polynomials are chosen based on the Galois Field (GF) theory, ensuring that the feedback function produces a maximum-length pseudo-random sequence. The presence of multiple non-adjacent terms in the polynomial enhances randomness, making LFSR-based test generators ideal for high-speed, low-area test pattern generation in modern VLSI design applications.

Generating high-quality test patterns with minimal hardware overhead is crucial for efficient fault detection in digitate 32-bit LFSR utilizes a maximal-length polynomial to generate a sequence of pseudo-random numbers, ensuring through fault coverage in digital circuits. Its deterministic nature allows for repeatability, making it highly effective for self-test applications in VLSI, FPGA, and ASIC designs. With high-speed operation and scalability, the LFSR enhances Built-In Self-Test (BIST) methodologies by eliminating the need for external test equipment, reducing testing complexity, and improving the overall reliability of digital systems.

For FPGA-based realization, a 32-bit Linear Feedback Shift Register (LFSR) was deployed on the Basys 3 FPGA, utilizing its LUT-based fabric for efficient pseudo-random sequence generation. The LFSR output is partitioned into two 16-bit segments, where the Lower Significant Bits (LSB) precede the Most Significant Bits (MSB) on the seven-segment display, ensuring a structured visualization of the sequence. A dedicated slide switch functions as reset control, forcing the LFSR output to a predefined high state when asserted, ensuring predictable

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initialization, controlled sequence repetition, and seamless integration into digital test pattern generation for BIST applications.

4. CIRCUIT UNDER TEST (CUT)

The Circuit Under Test (CUT) considered here is an XOR tree that performs a bitwise XOR operation on the 32-bit pseudo-random LFSR output to generate a single-bit CUT output. The XOR operation follows $A \oplus B = 1$ when inputs differ and $A \oplus B = 0$ when the inputs match. A hierarchical XOR tree structure was implemented using multiple 2-input XOR gates to systematically reduce the 32-bit input into a single-bit result. This combinational logic-based CUT ensures deterministic behaviour with minimal logic overhead, making it well suited for test pattern evaluation in BIST architectures.

The main advantage of using an XOR tree as the CUT is its simplicity in terms of both hardware implementation and Verilog-based RTL description. Because XOR is a purely combinational operation, Verilog's blocking assignments (=) can be efficiently used to update the CUT output instantaneously within the same procedural block. This ensures that the test pattern propagation and response evaluation occur in a single simulation cycle, thereby improving the predictability of the fault detection. The straightforward Boolean nature of the XOR function also minimizes the synthesis complexity, ensuring optimized resource utilization in FPGA or ASIC implementations. A 2-input XOR gate is typically realized using 6-transistor (6T) CMOS logic, balancing power and speed trade-offs while ensuring full swing voltage levels. In terms of power dissipation, the XOR tree exhibited dynamic power consumption ($P\_dyn = \alpha CV^2f$), where frequent switching contributed to energy loss. The hierarchical XOR tree structure results in a logarithmic delay scaling of O(logN), providing an efficient parallel reduction with minimal timing overhead. To address power constraints, low-power XOR gate implementations, such as transmission gate logic (TGL), pass-transistor logic (PTL), and FinFET-based XOR designs, are employed in sub-10 nm technology nodes.

From a VLSI design perspective, implementing the XOR tree as the CUT offers a high-speed evaluation with minimal control logic. The absence of sequential elements eliminates setup and hold time violations, thus simplifying the timing closure in high-frequency applications. In addition, the Verilog-based description benefits from direct synthesis into FPGA LUTs, ensuring area-efficient realization. With pipelining strategies or glitch-free XOR architectures, power and performance can be further optimized, making the XOR tree an effective choice for combinational CUT in self-test methodologies. In the Self-Test architecture, the XOR tree processes the 32-bit LFSR output and reduces it to a single-bit CUT output, which is either 1 or 0, based on the number of ones in the input pattern. If the count of ones is odd, the output is 1; if it is even, the output is 0, making it function as a parity checker for fault detection.

5. LOGIC DESIGN AND FAULT ANALYSIS

The self-test architecture is centered around a logic block that governs fault detection by analyzing the Circuit Under Test (CUT) output against a prestored reference. The comparator module plays a pivotal role in fault identification by comparing the CUT output with golden signatures generated during the fault-free phase. The test was divided into two phases. First, the fault-free system executes the test patterns generated by the LFSR and stores the corresponding golden CUT outputs in the memory. In the second phase, the same test patterns were reapplied, and the CUT responses were compared with the stored golden signatures. The comparator, which operates cycle-by-cycle, ensures accurate fault localization by detecting deviations between the expected and actual outputs.

To maintain precise fault detection and synchronization, dedicated hardware modules handle golden CUT storage and comparator-clock control. The golden CUT module stores reference data, whereas the comparator clock module ensures correct alignment with the LFSR-driven test sequence, preventing timing mismatches. The comparison logic relies on bitwise XOR operations, where a match signifies a fault-free operation, and a mismatch triggers a fault flag. This modular design enhances resource efficiency and ensures a structured, automated fault-detection process with high fault coverage and accuracy, thereby significantly reducing manual debugging efforts in VLSI testing. This approach makes it highly applicable to VLSI testing and validation environments, ensuring enhanced circuit robustness and reliability in FPGA-based BIST implementations.

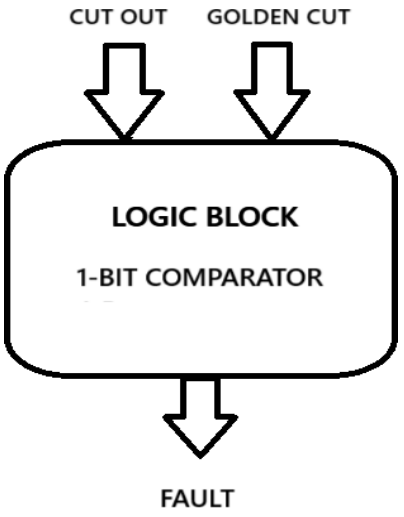

Figure 4: Logic block (1-bit comparator)

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6. SIMULATION RESULT AND ANALYSIS

In the proposed self-testing and fault-localization model, fault detection was efficiently achieved using a comparator module. The fault is manually injected by modifying the XOR logic in the Circuit Under Test (CUT) when the LFSR output reaches 32'h0000001B. In this specific test pattern, the CUT was altered to perform an XNOR operation instead of XOR, thereby modifying the expected output response.

The comparator module continuously compares the CUT output to the golden reference output (fault-free CUT response). When a deviation is detected, it asserts the fault signal (fault = 1), thereby identifying the occurrence of a fault and pinpointing the exact clock cycle and test pattern responsible for the failure. Unlike conventional BIST models, which focus solely on fault detection, the proposed approach localizes the fault, enabling a precise fault-diagnosis mechanism.

The simulation results of the proposed self-testing and fault-localization model validate its effectiveness for accurate fault detection and localization. The precise correlation between the test vector, CUT response, and fault flag assertion demonstrates the model's robust diagnostic capability in VLSI testing frameworks. The simulation waveforms provide a comprehensive validation of the proposed self-testing and fault-localization architecture. The 32-bit LFSR sequentially generates deterministic test patterns, which serve as stimuli for the Circuit Under Test (CUT). Throughout the initial test cycles, the CUT output (cut_out) remained consistent with the golden reference output (gold_out), indicating a fault-free operation. However, upon reaching the test vector LFSR = 32'h0000001B, the manually induced fault alters the logical behavior of the CUT, causing a mismatch between the CUT output and its golden reference counterpart. This discrepancy was precisely detected by the comparator module, leading to the assertion of the fault signal (fault = 1), thereby confirming the presence of an injected fault.

The simulation result of the self-test and fault localization system is shown below.

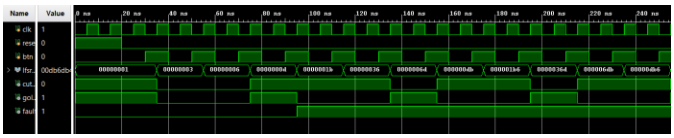

Figure 5: Simulation result of self-test system

Furthermore, the simulation results exhibit a precisely synchronized fault-localization mechanism that identifies the fault at the exact test pattern and clock cycle. Unlike conventional Built-In Self-Test (BIST) methodologies, which only determine the presence of a fault, this model effectively traces the fault back to the specific input vector responsible for the failure. The accurate correlation among the test vector, output deviation, and fault flag activation demonstrates the robustness of the proposed approach.

The FPGA Implementation of self-test system is shown in the below figure.

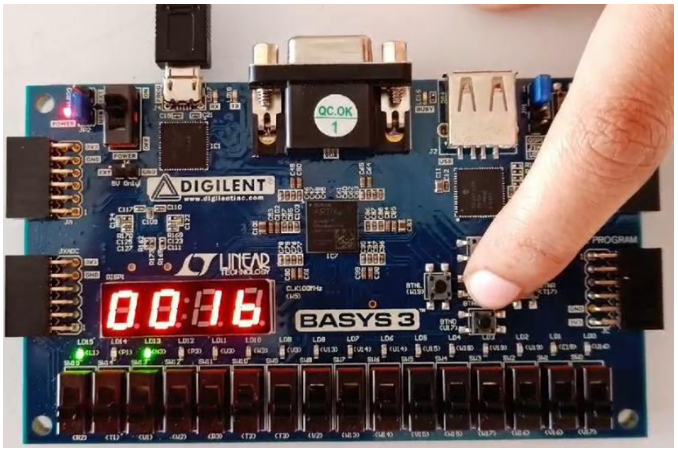

Figure 6: FPGA Implementation of self-test system

A structured approach was followed to develop the self-test system, beginning with the design and implementation of 16-bit and 32-bit Linear Feedback Shift Registers (LFSRs). These Pseudo-Random Number Generators (PRNGs) were constructed using maximal-length polynomials (primitive polynomials) to ensure high-quality test pattern generation. The 16-bit LFSR was primarily utilized for initial validation and small-scale testing, whereas the 32-bit LFSR was implemented for comprehensive fault detection and localization in complex circuits.

Following the successful integration of the LFSR-based PRNG, a self-test system was developed that incorporated a structured Built-In Self-Test (BIST) methodology. The LFSR outputs serve as deterministic test stimuli for the Circuit Under Test (CUT), enabling systematic fault injection and detection. The comparator module performed cycle-by-cycle evaluations, ensuring precise fault localization by referencing pre-stored golden CUT signatures.

The simulation result of 16-bit LFSR and 32-bit LFSR is shown in the below figures.

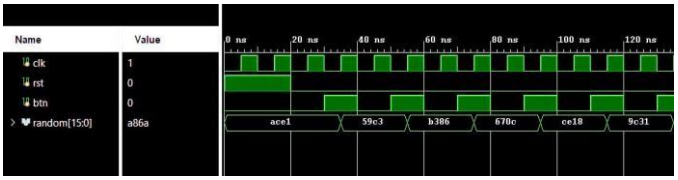

Figure 7: Simulation result of 16-bit LFSR

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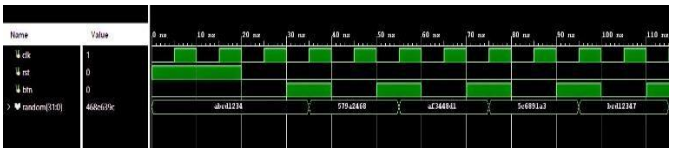

Figure 8: Simulation result of 32-bit LFSR

Through simulations and FPGA implementation, the proposed self-test and fault-localization model were successfully validated for accuracy, fault coverage, and hardware feasibility. The simulation ensured precise fault detection and localization, whereas the FPGA implementation demonstrated real-time functionality by mapping test outputs to LEDs and a seven-segment display. This confirmed the efficiency of the model in automated VLSI testing, making it a scalable and reliable solution for fault analysis and verification.

7. CONCLUSION AND FUTURE SCOPE

The proposed Enhanced Self-Test and Fault Localization System (STFLS) significantly improves VLSI fault detection by integrating a 32-bit Linear Feedback Shift Register (LFSR)-based Test Pattern Generator (TPG) with an XOR-tree-based Circuit Under Test (CUT) and structured fault comparison framework. Implemented in Verilog HDL and simulated using Xilinx Vivado, this methodology enhances fault isolation, system reliability, and scalability. By leveraging a structured fault detection and localization mechanism, STFLS ensures the accurate identification of faulty components in complex digital circuits, making it a valuable asset in semiconductor testing, embedded system debugging, and reliability analysis.

The system efficiently detects faults by generating pseudorandom test patterns using LFSR and comparing the expected outputs with observed CUT outputs using XOR and XNOR operations. This comparison mechanism enables precise fault identification and provides real-time insights into circuit behavior. To validate its effectiveness, the system was developed and simulated in Xilinx Vivado, ensuring a high accuracy and fault detection efficiency before FPGA deployment. Furthermore, the design was optimized to achieve low power consumption, high-speed performance, and minimal hardware overhead, making it suitable for applications in secure communication, fault-tolerant computing, and embedded systems.

In the future, STFLS can be extended to support adaptive self-test techniques that dynamically modify test patterns based on circuit behavior, improve test coverage, and reduce testing times. Additionally, integrating Machine Learning (ML)-based fault prediction models can further enhance the fault localization accuracy by identifying recurring failure patterns in VLSI circuits.

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