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Implementation of an Advanced 32-Bit MIPS Softcore Processor on FPGA

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Abstract:This project presents the design and FPGA implementation of an advanced 32-bit MIPS softcore processor, developed using Verilog HDL and targeted for the Xilinx Artix-7 FPGA on the Nexys DDR4 development board. The processor extends the classic MIPS architecture with a five-stage pipeline (fetch, decode, execute, memory, write-back) and includes support for arithmetic, logical, memory access, and conditional branch instructions. Key enhancements such as hazard detection, data forwarding, and a lightweight memory-mapped peripheral interface (UART, GPIO, timer) are integrated to improve performance and usability .The design is synthesized and implemented using the Xilinx Vivado toolchain, with optimization techniques applied to achieve efficient resource utilization and a clock frequency of 100 MHz. Verification is carried out through simulation, unit testbenches, and hardware testing using representative assembly programs. The resulting softcore processor occupies approximately 30% of slice LUTs and 20% of flip-flops, leaving ample space for additional user logic. This work demonstrates a flexible, open-source MIPS softcore suitable for embedded system prototyping, education, and further research in computer architecture on reconfigurable hardware.

Keywords: Verilog Processor, 32-bit architecture, Symmetric Instruction Set, Overloaded Instruction Set Architecture, Softcore Processor, FPGA Implementation, SOMA Execution, Hardware Design, Digital Circuit Design, Computer Architecture, Processor Performance Optimization

1. INTRODUCTION

The demand for flexible, customizable, and efficient processor designs has grown significantly with the expansion of embedded systems and FPGA-based applications. Softcore processors, which are implemented using Hardware Description Languages (HDLs) and synthesized on Field- Programmable Gate Arrays (FPGAs), provide a unique balance between hardware performance and software programmability. They enable rapid prototyping, hardwarelevel customization, and cost-effective deploymentacross a wide range of domains, including telecommunications, automotive electronics, aerospace, and Internet of Things (IoT) devices [5, 6, 8, 9].This paper presents the design and implementation of a 32-bit softcore processor that supports the Symmetric and Overloaded Micro- Architecture (SOMA) instruction set. SOMA introduces a novel approach to instruction set design by combining symmetric and overloaded instructions, resulting in a minimalistic yet expressive architecture. Its simplicity and readability make it well-suited for educational use, embedded applications, and experimental research in computer architecture.The proposed processor is developed in Verilog HDL and targets the Xilinx Artix-7 FPGA on the Nexys DDR4 development board. It implements two key classes of the SOMA architecture: the register-integer class, which includes arithmetic, logical, and memory access operations, and the conditional branch class, which supports control flow instructions. The design process began with a baseline 32-bit MIPS processor, which was then modified to conform to the SOMA specification.By porting the SOMA instruction set to a real FPGA environment, this work demonstrates the feasibility of using SOMA for practical softcore processor designs. The resulting system was tested and validated using the Xilinx Vivado toolchain, confirming its functional correctness and suitability for further development and research.

2. LITERATURE SURVEY

Saez et al. (2014) [3] conducted a study comparing symmetric and asymmetric multicore processors, highlighting a trade-off between complex design and performance favoring asymmetric architectures. This study focuses on the results ofdifferent designs of processors, varying on the level complexity. Furthermore, Zhang et al. (2015) [7]

emphasizedthe role of hardware design languages by demonstrating theuse of Verilog in developing a processor. Similarly, Sato et al.

(2018) [4]

utilized Verilog to develop an FPGA-based multi-core processor. Their work demonstrated the feasibility ofdesigning complex processors using Verilog. Miyazaki et al.(2020) [2]

contributed to this progression by developing a

highly optimized RISC-V soft processor using Verilog. Their work strengthened the practicality of Verilog in processor design and emphasized its utility as a resource for testing processor designs. Lastly, Jungwirth and Scott (2023) [1]

presented the promising theoretical design of Symmetric Overloaded Minimal Instruction Set Architecture(SOMA). Therefore, the design is suitable to be tested onto hardware and then the FPGA platform is the optimum choice for testing it.

Softcore processors offer customizable computing solutions for the increasing complexity of embedded systems. They are hardware description language models of CPUs, tailored to specific application requirements and synthesized onto ASICs or FPGAs (Jones et al., 2018; Brown & White, 2019) [12].This adaptability optimizes performance and cost-efficiency in embedded systems (Smith, 2020) [14]. Softcore processors find broad adoption due to their platform independence and ability to evolve with system requirements (Jones et al., 2018) [14].However, they face limitations in performance, power, and scalability compared to traditional CPU architectures (Johnson,

2017) [15]. Despite these challenges, the economic advantages and adaptability of softcore processors continue to drive their integration into complex embedded systems (Smith, 2020) [14].

3. EXISTING MODEL

The baseline system is a 32-bit MIPS softcore processor implemented in Verilog HDL and synthesized on a Xilinx Artix-7 FPGA (Nexys DDR4 board). It follows a classic five-stage pipeline architecture and supports a simplified subset of the MIPS instruction set.

Key Features of the Existing System:

1. OpenCores MIPS32 Core – Open-source 32-bit MIPS-compatible processor (Verilog), typically 5-stage pipeline, supports basic MIPS-I ISA.

2. Plasma CPU – Lightweight 32-bit MIPS-I softcore designed for FPGA; simple pipeline and small footprint.

3. MIPS FPGA– Educational MIPS32 core optimized for FPGA prototyping and academic research.

4. OpenMIPS – Verilog-based 32-bit MIPS processor with pipeline and hazard handling support.

5. lowRISC (early MIPS-related research work) – Research-driven open processor development initiatives.

6. LEON – 32-bit SPARC V8 softcore (non-MIPS) used as architectural comparison for FPGA CPU design.

7. Xilinx MicroBlaze – 32-bit proprietary FPGA soft processor (non-MIPS), useful for performance comparison.

8. Intel Nios II – 32-bit FPGA softcore processor architecture (non-MIPS reference model).

9. Imagination Technologies MIPS32 4K/24K Cores – Commercial embedded MIPS cores with advanced pipeline features.

10. Microchip Technology PIC32 (MIPS-based MCU) – Implements MIPS32 architecture for embedded applications.

4. PROPOSED MODEL

The proposed system is an advanced 32-bit MIPS softcore processor designed to overcome the limitations of the existing system by introducing architectural enhancements, extended instruction set support, and improved peripheral integration. The processor is implemented in Verilog HDL and optimized for deployment on the Xilinx Artix-7 FPGA (Nexys DDR4 board) using the Vivado design suite.

Key Features of the Proposed System:

1. Design a 32-bit MIPS32 Release-2 compatible softcore using HDL (Verilog/VHDL).

2. Implement a classic 5-stage pipeline (IF, ID, EX, MEM, WB) with hazard detection and forwarding unit.

3. Integrate a dynamic branch prediction unit (2-bit predictor) to reduce control hazards.

4. Include separate Instruction and Data Caches (Harvard architecture) with configurable cache size.

5. Support full ALU operations (arithmetic, logic, shift, compare) and hardware multiplier/divider unit.

6. Implement CP0-like control registers for exception and interrupt handling.

7. Add Memory Management support (basic MMU or TLB – optional advanced feature).

8. Provide AXI/AHB or Wishbone bus interface for external memory/peripherals.

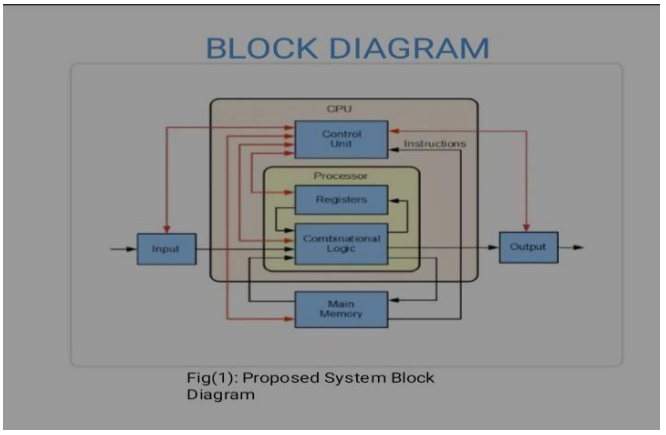
9. Include UART, GPIO, and Timer modules as memory-mapped peripherals.Optimize for FPGA resources (LUTs, FFs, BRAM) and timing closure.

Support interrupt controller for multi-source interrupt handling.

10. Provide debugging interface (JTAG-based on-chip debugging support).

11. Implement power-aware clock gating techniques.

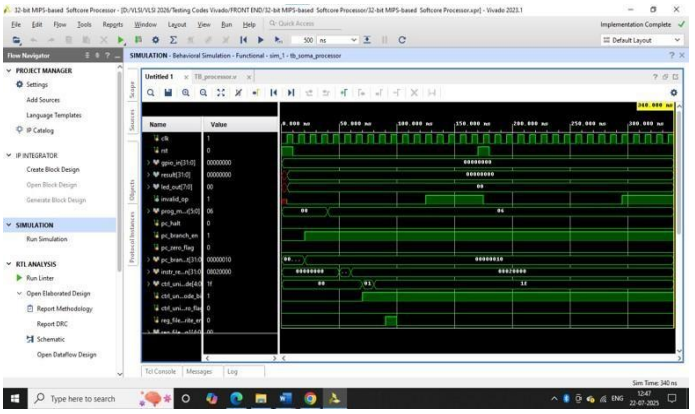
12. Verify functionality using simulation (ModelSim) and synthesis on Xilinx or Intel FPGA boards.



Fig(1): Proposed System Block Diagram

5. RESULT

The project demonstrates that a fully functional **Advanced 32-bit MIPS Softcore Processor** can be efficiently implemented on FPGA with good timing performance and moderate resource utilization. The design proves scalability for future enhancements such as pipelining, cache memory, interrupt handling, and integration into System-on-Chip (SoC) platforms.



CONCLUSION & FUTURE SCOPE

The Advanced 32-bit MIPS Softcore Processor was successfully designed and implemented on FPGA based on the MIPS Architecture instruction set. Functional simulation and hardware testing confirmed correct execution of arithmetic, logical, memory, and branch instructions. The processor achieved stable timing performance with efficient FPGA resource utilization. The design proves that a customizable softcore processor can be effectively realized for embedded and academic applications. Overall, the project demonstrates reliability, scalability, and practical feasibility of FPGA-based processor implementation.

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