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Implementation of SEC-DED-DAEC Codes using Mentor Graphics

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ABSTRACT

Correction of a single error Double Error Detection (SEC-DED) and Double Adjacent Error Correction (DAEC) are prominent error correction algorithms used in computer memory systems to detect and fix errors that arise during data transfer. In this research, we want to put these ideas into practice and assess how well they work through simulations and experiments. We will research the trade-offs between these strategies' efficiency and reliability and contrast them with other error correction techniques. Our research will involve designing and putting error detection and correction procedures into circuits and algorithms for DAEC and SEC-DED. We will also investigate other methods, including parallel processing and error checking mechanisms, to enhance the performance of these strategies. Our findings may also have applications in other domains where error correction is important, such as communication systems and medical equipment. They will help us understand and enhance error correction techniques used in computer memory systems.

INTRODUCTION

Data transmission and storage are becoming an essential element of daily life in the modern world. The probability of errors likewise rises as data is transferred and stored in greater quantities. These mistakes can corrupt data, which can cause system crashes or data loss. Data accuracy and integrity are guaranteed during transmission and storage using error correcting techniques. Correction of a single error Two common error correction methods used in computer memory systems are double error detection (SEC-DED) and double adjacent error correction (DAEC). Whereas DAEC can detect and correct up to two adjacent faults, SEC-DED can only detect and repair single-bit errors and double-bit errors. To guarantee data integrity and dependability, these approaches are applied in a variety of computer memory systems, including RAM and hard disc drives. We want to investigate and assess how well these error correction methods function in this project. For SEC-DED and DAEC, we will build and implement algorithms and circuits and analyse the trade-offs between their efficiency, dependability, and complexity. Our effort will provide light on how mistake correction methods in computer memory systems can be optimised and improved, and it may have applications in other areas where error correction is crucial.

1. Literature survey:

The book "Error Correction Codes" by Stephen B. Wicker and Shridhar Bhattacharyya offers a thorough introduction of numerous error correction code types, including SEC-DED and DAEC, and their applications in diverse disciplines. The SEC-DED technique is described in "Single Error Correction, Double

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Error Detection Codes for Memory" by Hamming, R. W., who also offers a mathematical demonstration of its efficacy in identifying and fixing mistakes in computer memory systems. The DAEC methodology is proposed in "A Double Adjacent Error Correction Technique for Memory Systems" by Yiqun Zhang and Graham A. Jullien, who also evaluate its effectiveness in comparison to existing error correcting techniques. The authors show that DAEC offers a greater level of reliability by successfully correcting faults in nearby memory cells. The performance of SEC-DED is compared to that of other error correction codes in terms of error detection and correction capabilities, memory requirements, and processing time in "A Comparative Analysis of SEC-DED Codes and Other Error Correction Codes" by Ahmad, F., et al. An SEC-DED code for error detection and correction in a memory system using Verilog HDL is designed and implemented in "Design and Implementation of SEC-DED Code for Error Detection and Correction in Memory System" by Kumar, P. and Sharma, A. According to Shrivastava, S. K., and Singh, V. K., "Double Adjacent Error Correction Method for Memories: A Novel Approach," a modified DAEC technique is suggested that may identify and fix multiple mistakes in adjacent memory cells, offering a better level of dependability than conventional DAEC. These studies highlight the significance and potency of SEC-DED and DAEC techniques for identifying and fixing mistakes in computer memory systems and offer insightful recommendations for their application and improvement.

Single Error correction-Double Error Detection:

Correcting a single mistake In computer memory systems, the Double Error Detection (SEC-DED) error correction technology is used to identify and fix data transmission mistakes. It is intended to both recognise and fix single-bit faults as well as recognise double-bit errors without necessarily fixing them. In SEC-DED, a code word is made by adding a second parity bit to the initial data bits. The total number of 1s in the code word is always even because of how this parity bit is calculated. If a single bit error happens during transmission, the parity bit can be utilised to locate the error and fix it. A double-bit error causes the parity check to fail, which results in the issue being identified but not fixed. Due to its ease of use and efficiency in identifying and fixing single-bit faults, SEC-DED is a well-liked and commonly utilised error correction technology. It is frequently utilised in fields including aerospace, the military, and medical devices where high dependability and data accuracy are essential.

Single Error Correction-Double Error Detection-Double Adjacent Error Correction:

Correction of a single error In order to find and fix errors that happen during data transfer, computer memory systems use double error detection (SEC-DED) and double adjacent error correction (DAEC). SEC-DED is intended to identify single-bit faults and fix them, as well as identify double-bit errors without necessarily fixing them. To make a code word, an extra parity bit is added to the initial data bits. If a single bit error happens during transmission, the parity bit can be utilised to locate the error and fix it. A double-bit error causes the parity check to fail, which results in the issue being identified but not fixed. Double-bit errors can be fixed when they occur in adjacent memory cells using the more sophisticated technique known as DAEC. This is accomplished by incorporating extra redundant bits into the data word and using a unique algorithm to identify and fix faults. In memory systems where neighbouring cell errors are likely to happen, DAEC is more sophisticated than SEC-DED but offers a better level of reliability. In computer memory systems and other applications where data quality and dependability are crucial, SEC-DED and DAEC are both commonly employed. They may greatly enhance the performance and

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lifetime of memory systems and are efficient at finding and fixing problems.

RESULTS:

- Schematic design of hamming code and outputs are verified.
- simulation waveforms of hamming code are observed.
- Schematic design of parity generator and outputs are verified.
- simulation waveforms of parity generator are observed.

Single error case

- Single error simulation waveforms are observed.
- Double error case
- Double error simulation waveforms are observed.
- Schematic design of SEC-DED decoding logic (no error) outputs are verified.
- Simulation waveforms of SEC-DED decoding logic (no error) are observed.
- Schematic design of encoder circuit of SEC-DED-DAEC outputs are verified.
- Simulation waveforms of encoder circuit of SEC-DED-DAEC are observed.
- Schematic design of decoder circuit of SEC-DED-DAEC outputs are verified.
- Schematic design of decoder circuit of SEC-DED-DAEC outputs are verified.
- Simulation waveforms of decoder circuit of SEC-DED-DAEC are observed.

(I)Simulation and schematic outputs:

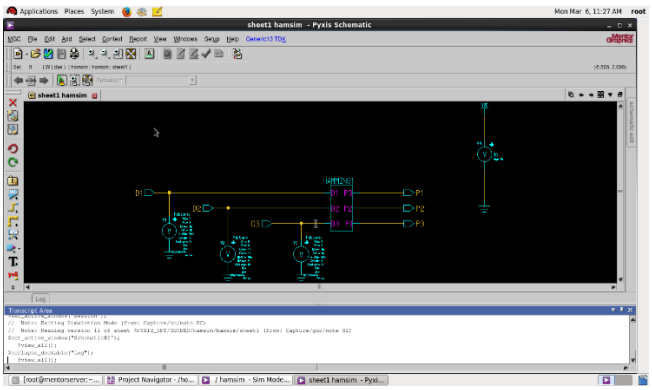

Fig-3.1.1: Schematic design of hamming code

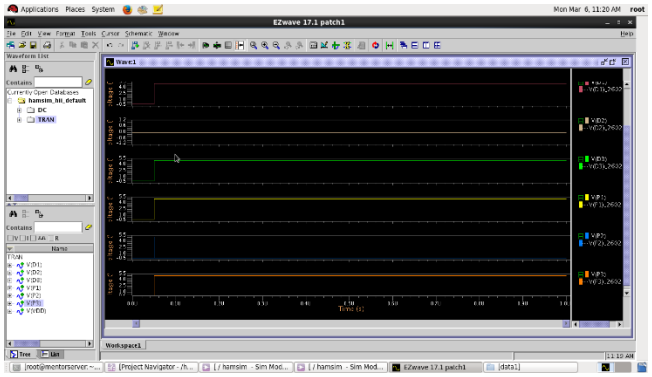

Fig-3.2.1: simulation waveforms of hamming code

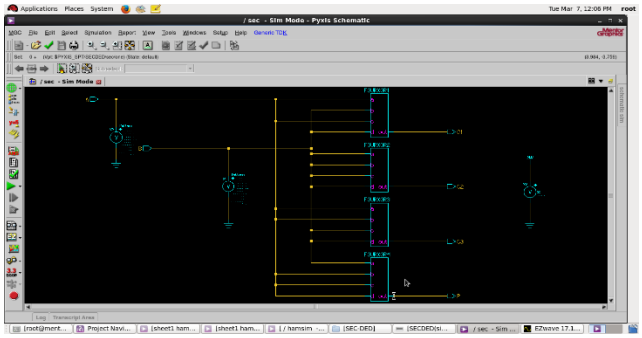

Fig-3.1.2: Schematic design of parity generator

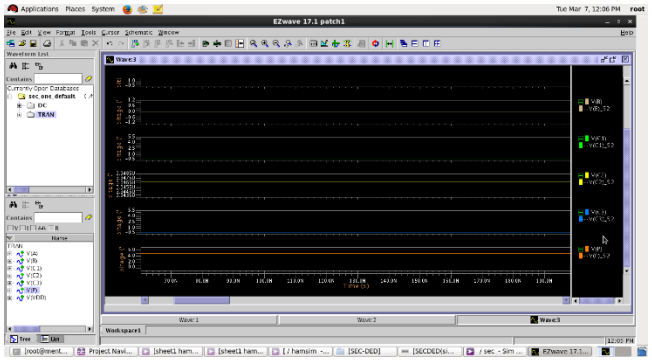

Fig-3.2.2: simulation waveforms of parity generator

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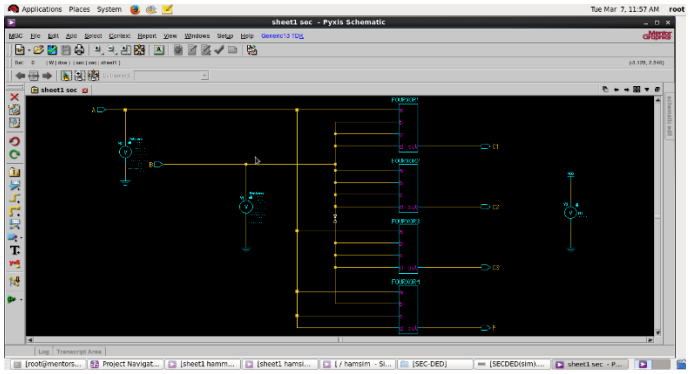

Fig-3.1.3: Single error

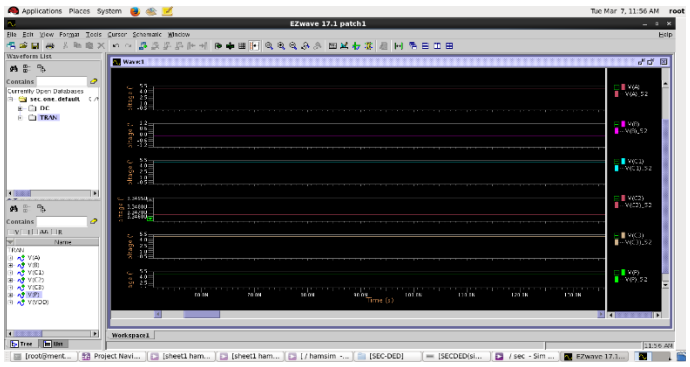

Fig-3.2.3: Single error simulation waveforms

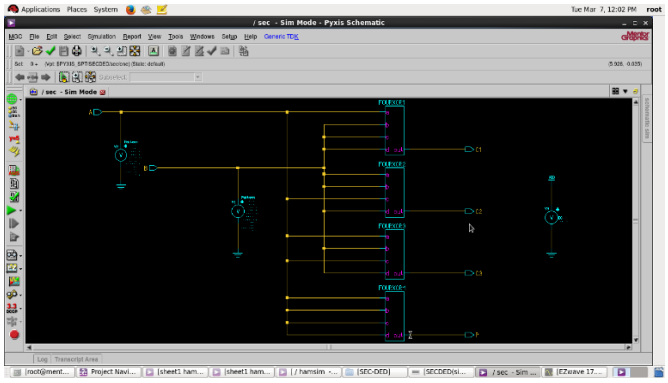

Fig-3.1.4: Double error

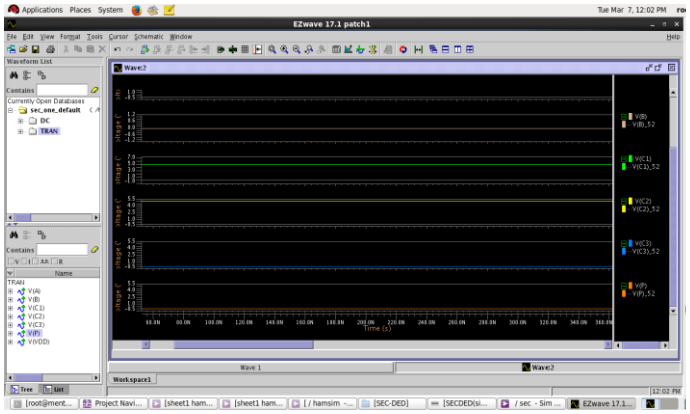

Fig-3.2.4: Double error simulation waveforms

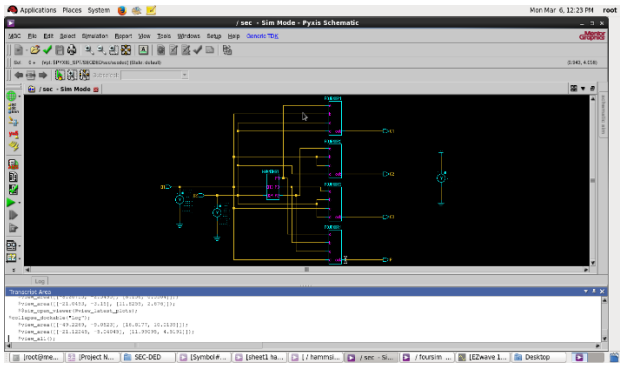

Fig-3.1.5: Schematic design of SEC-DED decoding logic (no error)

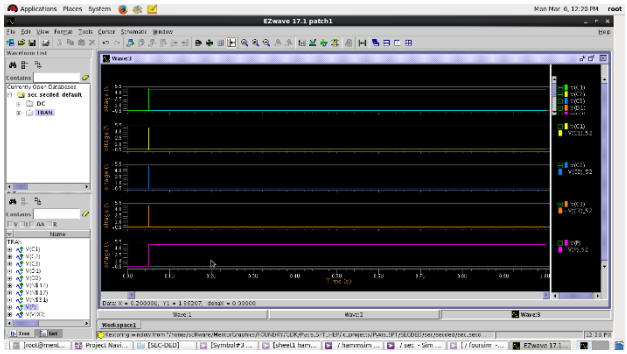

Fig-3.2.5: Simulation waveforms of SEC-DED decoding logic (no error)

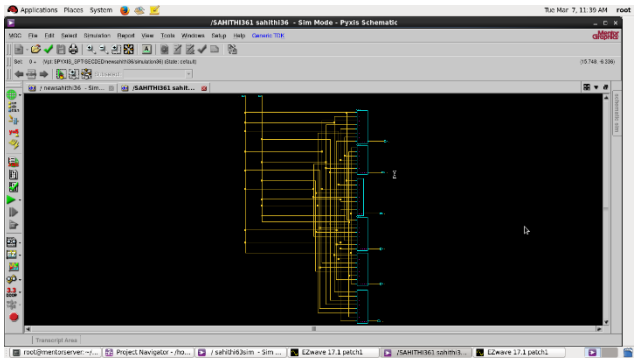

Fig-3.1.6: Schematic design of encoder circuit of SEC-DED-DAEC

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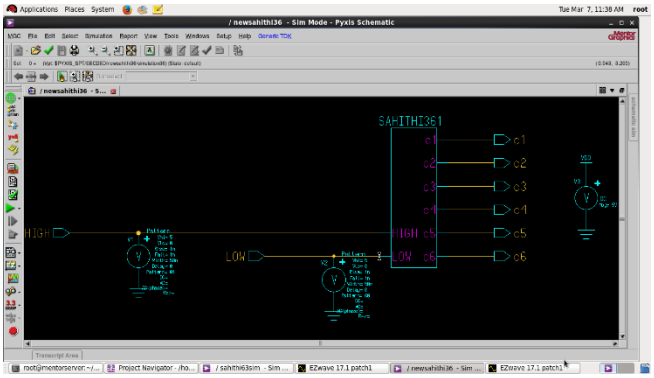

Fig-3.1.7: Schematic design of encoder circuit of SEC-DED-DAEC

Fig-3.2.6: Simulation waveforms of encoder circuit of SEC-DED-DAEC

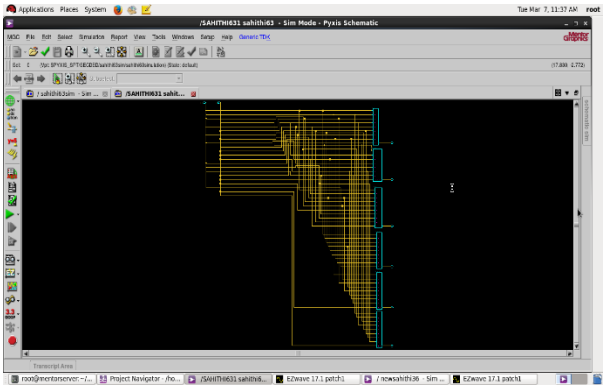

Fig-3.1.8: Schematic design of decoder circuit of SEC-DED-DAEC

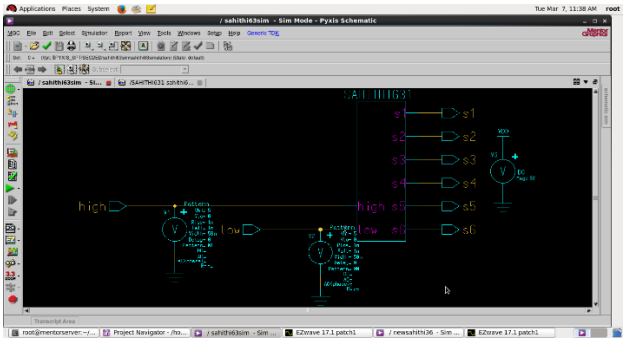

Fig-3.1.9: Schematic design of decoder circuit of SEC-DED-DAEC

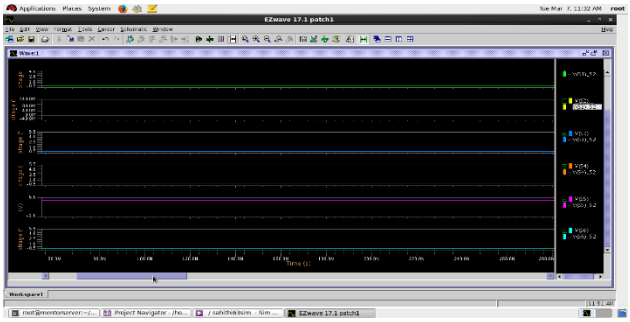

Fig-3.2.7: Simulation waveforms of decoder circuit of SEC-DED-DAEC

CONCLUSION:

In conclusion, two error correction approaches are employed in computer memory systems to find and fix faults that happen during data transmission: Single Error Correction Double Error Detection (SEC-DED) and Double Adjacent Error Correction (DAEC). SEC-DED is intended to identify single-bit faults and fix them, as well as identify double-bit errors without necessarily fixing them. Double-bit errors can be fixed when they occur in adjacent memory cells using the more sophisticated technique known as DAEC. In computer memory systems and other applications where data quality and dependability are crucial, SEC-DED and DAEC are both commonly employed. They may greatly enhance the performance and lifetime of memory systems and are efficient at finding and fixing problems. However, DAEC uses more memory resources and is more complicated than SEC-DED. Which error correcting method is employed depends on the requirements and limitations of the application. While DAEC offers a better level of dependability in memory systems where neighbouring cell faults are likely to occur, SEC-DED is a straightforward and efficient method for identifying and repairing single-bit mistakes. Overall, the employment of error correction methods like SEC-DED and DAEC can significantly boost the accuracy and dependability of data transfer in memory systems and is crucial in crucial applications

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including aerospace, defence, and medical equipment.

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