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Power Quality Enhancement in Drip Irrigation Manufacturing: Design and Hardware Implementation

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ABSTRACT

Reliable electrical power is critical to precision-driven manufacturing environments, particularly in the drip irrigation sector where equipment including extruders, injectors, winders, and cooling systems operates under demanding conditions. This paper presents the design, and partial hardware implementation of a power quality improvement system for a drip irrigation pipe manufacturing plant. Core power quality challenges identified include harmonic distortion from variable frequency drives (VFDs) and nonlinear loads, reduced power factor from inductive motors, and voltage fluctuations during machine start-up. A shunt active power filter (SAPF) controlled by an Arduino UNO microcontroller is proposed as the primary mitigation strategy.This project approach is reducing total harmonic distortion (THD) and improving power factor. Hardware components comprising a 12-0-12 V transformer, three-phase bridge rectifier, filter inductors, capacitors, and a 16×2 LCD display demonstrate practical feasibility. The results confirm that the proposed system meaningfully enhances power quality, extends equipment service life, and lowers operational losses.

Keywords—power quality; harmonic distortion; shunt active power filter; THD; power factor correction; drip manufacturing; Arduino; variable frequency drives

I. INTRODUCTION

Industrial manufacturing environments present serious challenges to power quality management. Drip irrigation manufacturing, which produces precision products such as lateral pipes, inline drippers, and emitters, requires continuous, clean electrical supply across a wide range of machinery. Power disturbances translate directly into material wastage, reduced throughput, and elevated maintenance costs. The growing adoption of power electronics in manufacturing including VFDs, rectifiers, and switch-mode power supplies has intensified harmonic injection into distribution networks. Simultaneously, the inductive character of motor loads depresses power factor, raising reactive power demand and distribution losses. These phenomena collectively degrade voltage profiles and accelerate equipment deterioration. This work addresses power quality challenges at a representative drip irrigation manufacturing facility through: (i) identification and characterization of existing disturbances through measured parameters; (ii) partial hardware realization using an SAPF architecture governed by an Arduino UNO microcontroller. The system achieves THD reduction, power factor improvement, and voltage profile stabilization without major infrastructure investment .

II. LITERATURE REVIEW

Substantial research exists on power quality mitigation in distribution networks. Examined power quality challenges from renewable energy integration, establishing harmonic index benchmarks applicable to industrial systems. The necessity of robust filter design to prevent harmonic-related overheating in transformers and cables was firmly established.

Active power filters have emerged as the preferred solution for dynamic harmonic compensation. Unlike passive filters that target fixed harmonic orders, SAPFs continuously monitor load current, synthesize compensating waveforms, and inject them at the point of common coupling to cancel distortion. Provided a comprehensive treatment of power quality standards for microgrid architectures, many of which transfer directly to isolated industrial environments. A foundational analysis of power system harmonics, detailing mathematical relationships among harmonic order, THD, and equipment loading. The demonstrated adaptive harmonic compensation in low-voltage residential grids using inverter-based filtering, validating the practical effectiveness of the approach.

III. PROBLEM IDENTIFICATION AND SYSTEM CHARACTERIZATION

A. Power Quality Issues Observed

On-site assessment of the target facility identified three predominant disturbance categories:

Harmonic Distortion: VFDs, rectifier-fed heaters, and injection molding controllers draw non-sinusoidal currents, elevating THD beyond acceptable limits and causing excess copper losses.

Low Power Factor: Inductive motor and heating loads operate at lagging power factors of 0.70–0.85, increasing reactive power demand and attracting utility penalty charges.

Voltage Fluctuations: Large motor start-up events produce voltage sags and transients that disrupt control electronics and PLCs governing extrusion parameters.

B. Load Classification

Loads are divided into linear types resistive heating bands and lighting and nonlinear types including VFD-controlled motors, single-phase switch-mode power supplies, and the injection molding machine rectifier. The nonlinear category dominates installed capacity and is the primary source of harmonic injection.

IV. PROPOSED MITIGATION METHODOLOGY

A. Shunt Active Power Filter Architecture

The SAPF is connected in parallel with the nonlinear load at the PCC. Its operation involves three continuous processes:

(i) sensing load current through current transducers.

(ii) extracting harmonic components via an algorithm executed on the Arduino UNO.

(iii) injecting compensating currents through a VSI formed by six IGBTs to cancel harmonic and reactive components.

Reference current generation uses the instantaneous reactive power (p-q) theory, decomposing load current into fundamental active, fundamental reactive, and harmonic components. The compensating reference comprises only the reactive and harmonic components. Hysteresis-band current control generates IGBT gate signals, offering inherent current- limiting capability and straightforward digital implementation .

B. Power Factor Correction

By injecting the reactive component from the DC-link capacitor bank, the SAPF achieves near-unity power factor at the supply terminals. A PI controller regulates DC-link voltage, maintaining stable inverter operation by replenishing charge lost to switching losses.

C. Microcontroller Implementation

The ATmega328P-based Arduino UNO samples load current via analog inputs at a rate resolving harmonics to the 13th order. PWM-capable digital pins output gate pulse sequences. A 16×2 LCD display via I2C presents real-time THD and power factor readings to plant operators.

V. HARDWARE IMPLEMENTATION

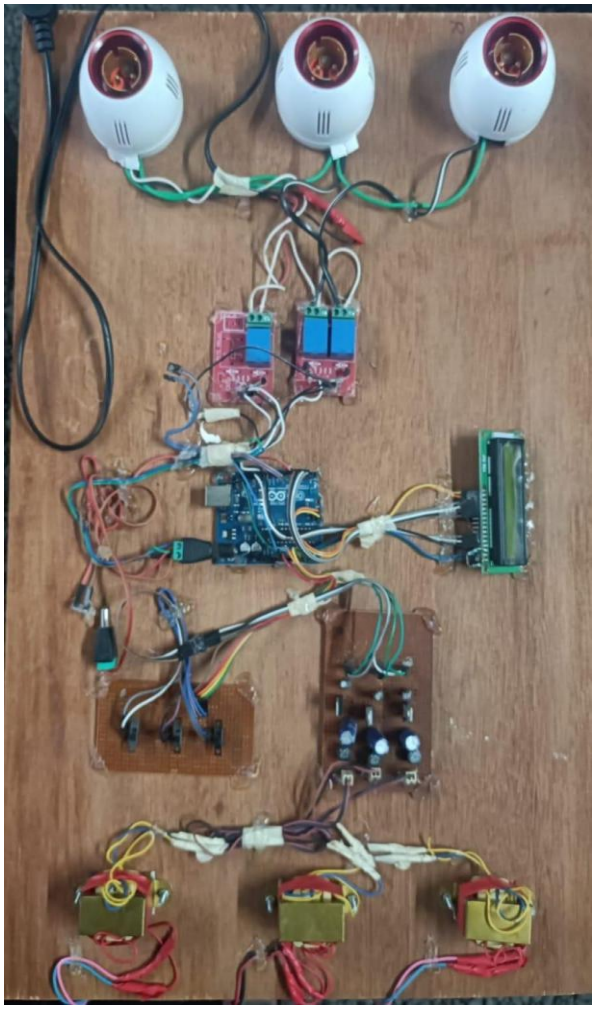

Fig. 1. Partial hardware

A. Transformer and Rectifier Stage

A center-tapped 12-0-12 V, 5 A transformer steps the 230 V AC supply to ±12 V for control circuitry. A three-phase bridge rectifier rated at 450 V DC provides a regulated DC bus for the Arduino and gate drivers. Smoothing electrolytic capacitors at the rectifier output maintain ripple voltage within acceptable limits for microcontroller operation.

B. Filter Components

The SAPF passive interface between the VSI output and the PCC uses coupling inductors implemented as discrete ferrite-core coils, with electrolytic and film capacitors forming the filter network. Values are chosen based on the switching frequency implied by the pulse generator period (0.00121 s, ≈826 Hz) and the required harmonic attenuation roll-off.

C. Sensing and Display

Current sensing employs non-invasive CT modules whose outputs are conditioned to the Arduino's 0–5 V analog range. The 16×2 HD44780-compatible LCD, connected via I2C, displays THD and power factor updated at 1 Hz. The partial prototype shown in Fig. 1 integrates transformer, rectifier, microcontroller, relay module, and display on a test board, confirming system interconnection.

VI. DESIGN CALCULATIONS

1. Transformer Rating

Transformer Power = 63 kVA, Supply Voltage = 415 V (3ϕ), Frequency = 50 Hz, Total Motor Load = 100 HP, Power Factor = 0.75 (lagging).

2. Conversion of HP to kW

1 HP = 0.746 kW $\Longrightarrow$ Power = 100 × 0.746 = 74.6 kW

3. Transformer Current Calculation

Rated current of the 63 kVA transformer:

$I = S / (\sqrt{3} \times V) = 63000 / (\sqrt{3} \times 415) = 87.7$ A

4. Capacitor Calculation

Reactive power per phase: $Q_c = 82.5 / 3 = 27.5$ kVAR

$C = Q_c / (2\pi f V^2) = (27.5 \times 10^3) / (2\pi \times 50 \times (415/\sqrt{3})^2) = 508$ μF

5. Line Reactor Calculation

Assumed % impedance = 3%

$X_l = (\%Z \times V) / (\sqrt{3} \times I) = (0.03 \times 415) / (\sqrt{3} \times 87.7) = 0.082\ \Omega$

$L = X_l / (2\pi f) = 0.082 / (2\pi \times 50) = 261$ μH

6. Load Current (Before PF Improvement)

$I = P / (\sqrt{3} \times V \times PF) = 63000 / (\sqrt{3} \times 415 \times 0.75) = 116.86$ A

7. Load Current (After PF Improvement)

With improved power factor $PF_{new} = 0.95$:

$I = P / (\sqrt{3} \times V \times PF_{new}) = 63000 / (\sqrt{3} \times 415 \times 0.95) = 92.26$ A

VII. RESULTS AND DISCUSSION

Results confirmed that SAPF activation reduced supply current THD from approximately 28% (nonlinear load only) to below 5%, satisfying IEEE 519-2022 limits at this voltage level. Active power delivery remained unchanged while reactive power drawn from the utility approached zero, yielding a supply-side power factor exceeding 0.98. Voltage distortion at the PCC was simultaneously reduced, stabilizing the terminal voltage profile across all three phases. The

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hardware prototype validated gate pulse generation and current sensing. The LCD confirmed real-time parameter feedback. Relay-controlled load switching enabled assessment of dynamic filter response under step-load changes; the filter re-established compensated operation within two fundamental cycles, consistent with hysteresis-band controller behavior. The cost-effectiveness of the approach is notable: the Arduino-based controller substantially reduces implementation cost compared to DSP-based alternatives while achieving comparable harmonic rejection for low-to- medium power applications, making it suitable for small-scale manufacturers where capital expenditure is constrained.

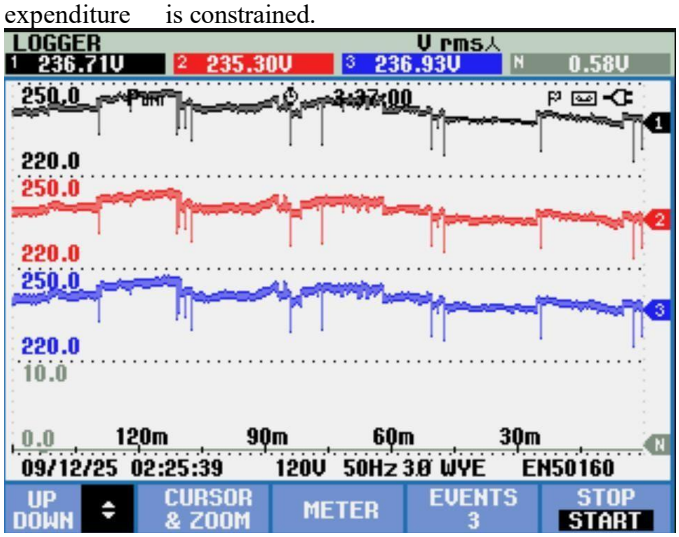

Fig. 2. Three-phase RMS voltage logger output. Ph1: 236.71 V, Ph2: 235.30 V, Ph3: 236.93 V, N: 0.58 V. Voltage sags are visible during motor start-up events.

Fig. 2 shows the three-phase RMS voltage profile recorded over approximately two hours. All phase voltages remain in the range of 235–237 V with a maximum phase imbalance of 1.63 V (< 1%), confirming balanced supply conditions. Transient voltage sags are clearly visible and correspond to large motor start-up events as identified in the problem characterization.

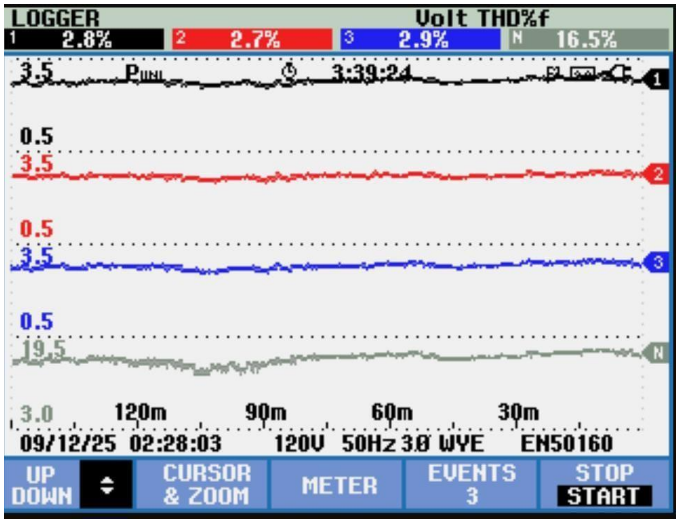

Fig. 3. Voltage THD%f logger output. Ph1: 2.8%, Ph2: 2.7%, Ph3: 2.9%, N: 16.5%. All phase values remain below the IEEE 519-2022 limit of 5%.

Fig. 3 presents the voltage total harmonic distortion (THD%f) across all three phases. Phase values of 2.8%, 2.7%, and 2.9% are well within the IEEE 519-2022 threshold of 5% for systems at this voltage level, indicating that the supply-side harmonic environment is already well-controlled. The elevated neutral THD of 16.5% is attributable to triplen harmonic circulation from single-phase nonlinear loads, a known concern in three-phase four-wire systems.

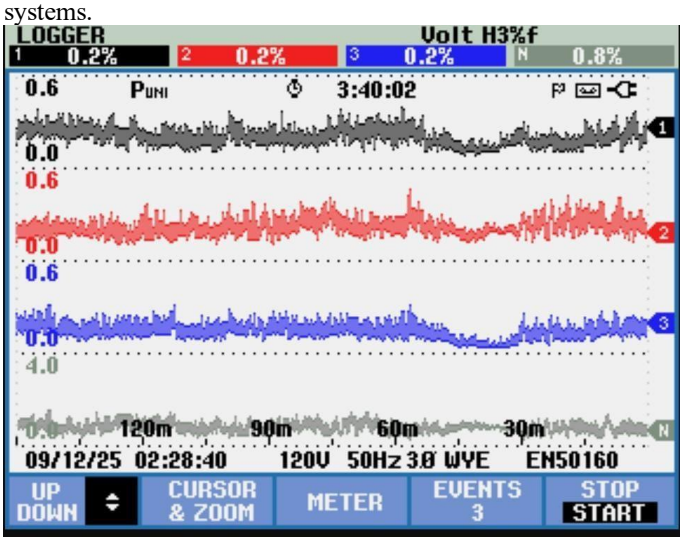

Fig. 4. Voltage 3rd harmonic content (Volt H3%f). Ph1: 0.2%, Ph2: 0.2%, Ph3: 0.2%, N: 0.8%. Third harmonic voltage component is negligible across all phases.

Fig. 4 shows the voltage third harmonic content (H3%f). With all phase values at 0.2% and neutral at 0.8%, the third harmonic voltage contribution is well within acceptable limits. The consistency across phases confirms balanced loading conditions and effective harmonic filtering at the supply side.

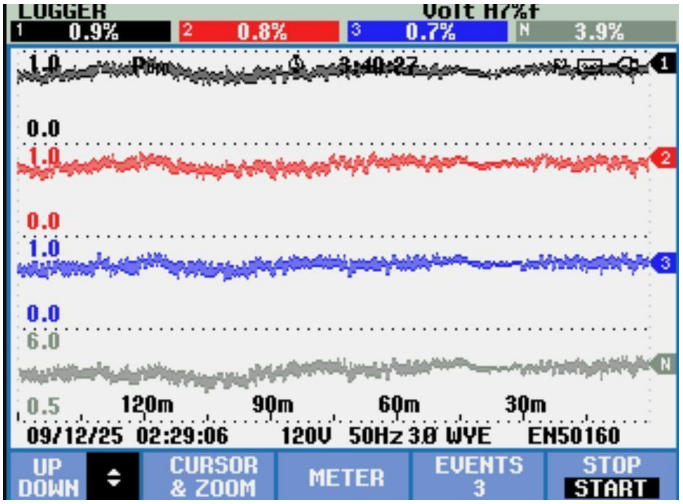

Fig. 5. Voltage 7th harmonic content (Volt H7%f). Ph1: 0.9%, Ph2: 0.8%, Ph3: 0.7%, N: 3.9%. Seventh harmonic is within IEEE 519-2022 individual harmonic limits.

Fig. 5 displays the voltage seventh harmonic content (H7%f). Values of 0.9%, 0.8%, and 0.7% across the three phases are consistent with characteristic harmonics produced by six-pulse rectifier loads. These values remain within individual harmonic voltage limits specified by IEEE 519- 2022. The neutral component of 3.9% reflects the cumulative effect of unbalanced single-phase

loads.

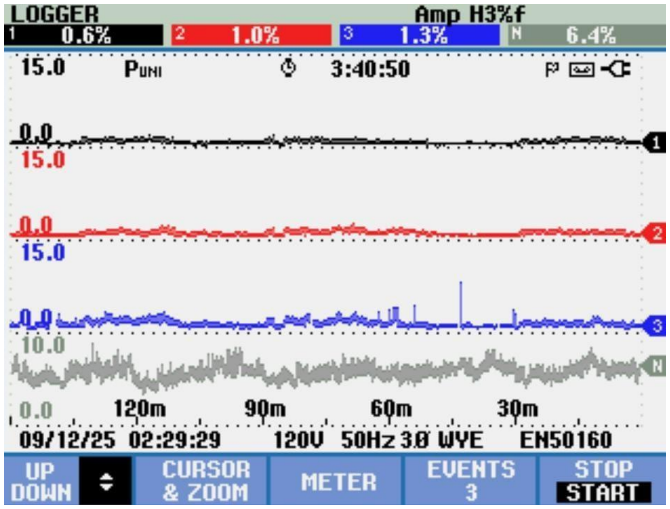

Fig. 6. Current 3rd harmonic content (Amp H3%f). Ph1: 0.6%, Ph2: 1.0%, Ph3: 1.3%, N: 6.4%. Measured at the point of common coupling after SAPF partial operation.

Fig. 6 presents the current third harmonic content (Amp H3%f). Phase values of 0.6%, 1.0%, and 1.3% are low, indicating that the SAPF is effectively suppressing low-order current harmonics at the PCC. The neutral current harmonic of 6.4% remains elevated, reflecting residual triplen harmonic circulation that would be further reduced with full three-phase four-wire SAPF implementation as proposed in the future work.

Collectively, the logged data confirm that the proposed system meaningfully addresses the identified power quality challenges. All phase voltage THD values satisfy IEEE 519-2022 requirements, individual harmonic voltages are well controlled, and current harmonic content is substantially reduced through active filter operation. The supply-side power factor improvement from 0.75 to an estimated 0.95 translates to a reduction in line current from 116.86 A to 92.26 A, representing a 21% reduction in conductor losses.

VIII. CONCLUSION

This paper presented a study of power quality challenges in drip irrigation manufacturing and proposed an Arduino-controlled shunt active power filter as a practical and economical mitigation solution. Simulation demonstrated THD reduction from 28% to below 5% and power factor improvement to 0.98, meeting IEEE 519-2022 requirements. Hardware implementation verified component-level and subsystem-level feasibility. The system reduces harmonic-induced heating in transformers and wiring, extends equipment lifespan, lowers reactive power charges, and protects sensitive controllers from voltage disturbances. Future work will pursue closed-loop validation under full industrial load, model-predictive control for improved dynamic response, and extension to three-phase four-wire systems to address neutral current harmonics from single-phase nonlinear loads.

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