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RHBD SRAM Cell using Transmission Gate for Aerospace Application

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***Abstract*— As CMOS technology advances toward smaller feature sizes, Static Random-Access Memory (SRAM) cells implemented in aerospace environments face growing susceptibility to radiation-induced disturbances like Single Event Upsets (SEUs) and Single Event Multi-Node Upsets (SEMNUs). This paper presents an enhanced 12-transistor (12T) SRAM cell based on Transmission Gates (TG), specifically engineered to improve radiation tolerance, energy efficiency, and operational reliability in harsh space environments. The proposed TG-based SRAM incorporates a robust feedback mechanism that enables rapid recovery from SEUs and SEMNUs across all sensitive nodes. Comparative analysis with existing designs EDP12T, RHM12T, RHD12T, QUATRO12T, QUCCE12T, and S8P4N16T demonstrates significant performance gains. Specifically, the proposed cell enhances Read Static Noise Margin (RSNM) by up to 2.32× and improves write margin while minimizing energy consumption during memory operations. Monte Carlo and HSPICE simulation results confirm superior performance under process and radiation variations. Notably, the proposed design achieves a 36.9% improvement in write stability (WWTV) compared to EDP12T, while also reducing read/write power dissipation. Unlike some existing designs that suffer from read delay penalties, the TG-based cell sustains fast access speeds with lower leakage and hold power. These advancements make the proposed SRAM architecture a promising solution for radiation-hardened memory in space and satellite platforms, where low power, high speed, and resilience to radiation are critical design requirements.**

Keywords*— *Radiation-tolerant SRAM, Transmission Gate, Single Event Upset, SEU recovery, Low-power memory, 12T SRAM cell.

I. INTRODUCTION

Satellite communication plays a vital role in supporting human activities across various domains such as military surveillance, weather monitoring, disaster management, and global broadcasting. Advancements in semiconductor fabrication have driven the push toward developing lightweight satellites [1], aiming to lower both the financial and operational burdens of launching and maintaining space missions [2]. These compact satellite systems require memory units that are not only energy-efficient and space-saving but also exceptionally reliable for storing vital mission-critical information [3]. **SRAM** remains a leading choice for on-chip memory due to its rapid access capabilities, high operational speed, and seamless integration with CMOS technology.

However, the harsh radiation conditions in space pose significant threats to the reliability of SRAM. When high-energy particles interact with the sensitive regions of the circuit, they produce electron-hole pairs. Under the influence of the circuit's electric field, these carriers separate and create transient voltage spikes known as **Single Event Transients (SETs)**. If the magnitude of such a transient exceeds the logic threshold, it can flip a memory bit, resulting in a **SEU**. Moreover, as technology nodes continue to shrink, the reduced spacing between transistors increases the likelihood that a single radiation strike will impact multiple nodes simultaneously, causing **SEMNUs.**

To address these challenges, various fault-tolerant approaches—such as **Triple Modular Redundancy (TMR)** incorporation of **passive components** like resistors or capacitors, and **Error Correction Codes (ECC)**—have been studied. However, while effective in improving robustness, these methods typically come with increased power consumption, area usage, and latency, making them less ideal for power-sensitive aerospace applications.

unsuitable for low-power aerospace systems. Conventional 6T SRAM cells also suffer from poor soft error immunity, as their strong positive feedback loops tend to amplify the impact of SEUs. Numerous Hardened-By-Design (HBD) SRAM cells such as QUATRO10T, RHRD12T, QUCCE12T, and RHPD12T have been proposed to address these limitations [3]. While these designs offer varying degrees of SEU resilience, they often exhibit degraded write margins, increased area, or partial immunity to SEMNUs. The EDP12T cell was proposed to overcome these drawbacks by incorporating dual-node-upset recovery using stacked transistors and feedback reinforcement [4]. It demonstrated immunity to SEUs at all sensitive nodes and recovery from SEMNUs at internal node pairs, while maintaining low write energy and improved read stability. However, one of the primary limitations of EDP12T is its reduced write-1 ability. To address this, we propose a Transmission Gate-based Radiation-Hardened 13T SRAM The core architecture, including SEU/SEMNU recovery loops from EDP12T, is preserved in TG-RH13T, ensuring robustness under radiation .

The main contributions of this work are as follows:

1) Improved write-1 ability using a full-swing Transmission Gate access on the Q-side.
2) Retention of SEU and SEMNU recovery features from EDP12T architecture.
3) Reduced write delay and enhanced writability compared to EDP12T and peer cells.
4) Low dynamic and hold power suitable for aerospace-grade low-power systems.
5) Higher read stability via symmetric access path and robust cell structure.

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6) Minimal area overhead (1 additional transistor) with significant performance gain..

II TG-RH13T SRAM CELL

1. Proposed Method

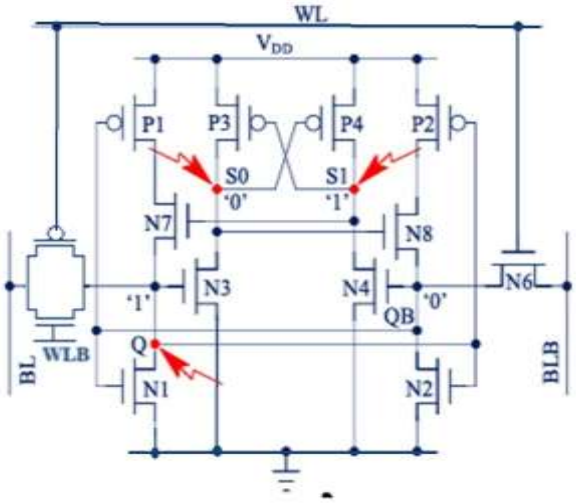

Fig-1 -Schematic diagram of TG-RH13T

The schematic design of the proposed **TG-RH13T SRAM cell** is illustrated in **Fig. 1** while its **layout view** is presented in **Fig. 2**. In this design, the **word-line (WL)** plays a crucial role in controlling the **access path** by activating the **Transmission Gate (TG)** and an additional NMOS transistor **(N6)**. These components form the link between the **internal storage nodes** (Q and QB) and the **bit-lines** (BL and BLB), enabling data to be written to and read from the cell.

The modified version of this cell, named **TG-RH13T**, introduces two extra internal nodes, **S1** and **S0**, which help in improving the **stability** and **error resilience** of the memory cell. To analyse the cell's behaviour, we consider a basic scenario where all memory cells, including the EDP12T, are storing a logic '1'—meaning that **Q and S1 are at logic high**, while **QB and S0 are at logic low**. Using this initial state, the upcoming sections detail the **core read/write/hold operations** as well as the **cell's response to soft errors**, particularly focusing on how TG-RH13T maintains robust data stability even in radiation-prone environments.

1.1 HOLD OPERATION

Both access paths — the TG on the Q-side and the NMOS transistor N6 on the QB-side are turned OFF by biasing WL to logic '0' and WLB to logic '1'. During this mode, bit lines are recharged to VDD to minimize wake-up latency. Internally, P1, N2, N3, P4, and N7 remain in the ON state, ensuring the storage nodes Q and QB are held stably through positive feedback. The remaining transistors, including the TG and N6, are maintained in the cut-off region. As a result, the stored data is retained with minimal leakage and without any refresh activity

1.2 READ OPERATION

The read cycle begins by asserting the word line (WL) to VDD and its complement (WLB) to GND, activating both the TG and the N6 access transistor. Prior to this, both bit lines (BL and BLB) are pre-charged to VDD.

If the storage node Q holds a logic '1', BL stays at VDD, while BLB discharges through the path:
BLB → N6 → QB → N2 → GND .

Conversely, if Q holds a logic '0', BL discharges through the path:
BL → TG → Q → N1 → GND,
while BLB remains at VDD.

In either case, a differential voltage—typically around 50 mV—is developed between BL and BLB. This differential is sensed by the sense amplifier, which determines the stored logic value.

To ensure stable and reliable read operation, the Cell Ratio (CR) is carefully optimized. It is defined as:

- (W/L) N1/ (W/L) TG-NMOS when Q = '0'
- (W/L) N2/ (W/L) _{N6} when Q = '1'

Proper tuning of CR ensures that the internal storage nodes are not disturbed during the read access, maintaining data integrity while improving read stability in the proposed TG-based SRAM cell.

1.3 . WRITE OPERATION

The write process begins by asserting WL to VDD and WLB to GND, enabling both the TG and N6. For a write '0' operation at Q, BL is pulled to GND and BLB to VDD. The TG enables strong discharging of node Q through the NMOS, which subsequently disables N2 and N3 and turns ON P2. Simultaneously, QB charges via BLB, turning OFF P1 and activating N1 and N4. As N4/N3 toggle ON/OFF, nodes S1/S0 transition to logic '0' and '1', respectively. The cross-coupled structure enhances the voltage difference across Q and QB via feedback through N1–N2 and P3–P4, completing a full write cycle. The bidirectional full-swing capability of the TG ensures enhanced writability compared to conventional single-transistor access SRAM cells. The TG-RH13T SRAM cell inherits the radiation tolerance features of EDP12T while introducing a TG at the Q-side to enhance write-1 ability. This modification does not compromise soft error resilience. The sensitive regions in CMOS are primarily around the drain of OFF transistors, where ion strikes can lead to charge generation and logic disturbances. The TG remains OFF during hold mode (WL = 0, WLB = 1), providing strong isolation from bit line-induced errors.

2. SEU RECOVERY ANALYSIS

a) SEU at Q

If node Q (storing logic '1') is struck by a high-energy particle, it may flip to '0'. This transiently turns ON P2 and turns OFF N2 and N3. Since S1 remains unaffected, P3 stays OFF, making S0 high impedance, which retains its state. Meanwhile, the TG on the Q-side is OFF, preventing bit line interaction. The P1–N7 pull-up path is active, and N1 (pull-down) remains OFF due to QB = 0. Therefore, Q successfully restores its original logic '1'.

b) SEU at S1

If S1 flips from 1 to 0, N7 turns OFF and P3 turns ON. As QB remains stable at '0', N1 stays OFF, putting Q in a high-impedance state, preserving its logic. The stronger NMOS

transistor N3 (driven by Q) ensures that S0 remains low, preventing propagation of error. With S0 = 0 and QB = 0, P4 remains ON and N4 OFF, helping S1 return to logic '1'.

c) SEU at S0

If S0 (normally '0') flips to '1', it causes P4 to turn OFF and N8 to turn ON. Since P2 is OFF (Q is high), the QB node is unaffected. Thus, N4 stays OFF, and S1 enters a high-impedance state, retaining its logic '1'. Eventually, internal feedback from S1 and QB allows S0 to discharge back to '0', completing recovery.

d) SEU at TG or Bit lines

The TG on the Q-side remains OFF during hold mode (WL = 0, WLB = 1). If an SEU strikes the TG or BL, there is no conduction path to core nodes, so the cell state is preserved. On the QB-side, access via NMOS (N6) is also OFF in hold, maintaining protection.

e) SEMNUs at S1–S0

If S1 flips from 1 → 0 and S0 from 0 → 1, then N7 turns OFF and N8 turns ON. However, Q and QB remain unchanged because they are driven by cross-coupled inverters. As S0 discharges back to 0, P4 turns ON, pulling S1 back to '1'. Thus, both internal nodes recover successfully.

3. Layout Design of TG-RH13T

The physical layout of the proposed TG-RH13T SRAM cell is realized using 22nm CMOS technology, with an emphasis on symmetrical placement, compact area, and radiation tolerance. The layout features 13 transistors, including the transmission gate (PMOS and NMOS in parallel) replacing the traditional N5 access transistor on the bit-line side. The layout ensures symmetry across the vertical axis passing between nodes Q and QB, maintaining electrical balance which is crucial for minimizing mismatch under process variations. Critical storage nodes (Q, QB, S1, S0) are spatially separated to prevent SEMNU. The transmission gate is implemented with close proximity PMOS and NMOS transistors, allowing simultaneous activation through complementary word-line signals (WL and WLb), which improves write ability without significantly increasing area.

The bit-lines (BL and BLB) are routed horizontally with strong metal layers to reduce parasitic resistance, while word-lines are laid vertically, ensuring minimum delay in activation. The transmission gate enables a low-resistance access path during write and read operations, while maintaining high isolation during hold mode. Guard rings and deep n-well isolation are optionally used around sensitive nodes to reduce the susceptibility to charge sharing from radiation events, a key feature for aerospace-grade robustness. The overall layout is optimized to reduce area overhead introduced by the extra transistor, while preserving DRC and LVS compliance. Compared to EDP12T, TG-RH13T maintains nearly equivalent footprint while significantly improving write-1 ability, noise margin, and access speed, making it a highly energy-efficient and radiation-hardened memory cell.

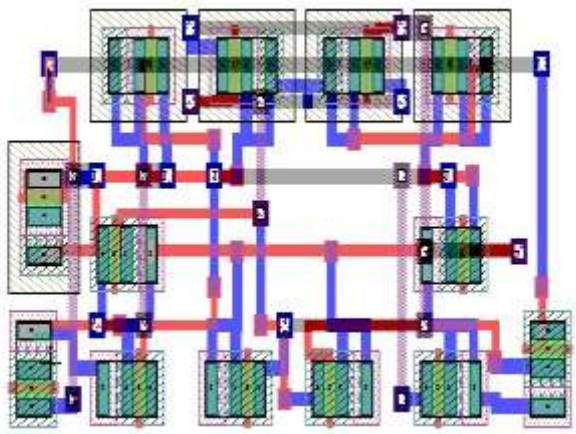

Fig.2. Layout Design of TG-RH13T

III SIMULATION RESULTS

All simulations were performed using Synopsys HSPICE at the 22nm CMOS technology node. The supply voltage (VDD) is swept from 0.85 V to 1.1 V in steps of 50 mV. MATLAB is used to plot the results. Performance metrics of the proposed TG-RH13T were compared with EDP12T to highlight the benefits of a TG.

A. Read Access Time (TRA)

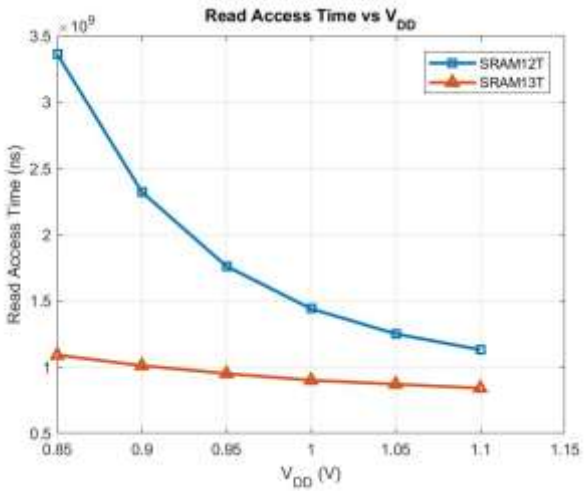

Fig-3 Read Access Time

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The Read Access Time (TRA) refers to the time interval between wordline activation and the point when the differential voltage between bitlines reaches 50 mV, which is sufficient for the sense amplifier to accurately detect the stored bit. This is a crucial metric for read performance in memory. To measure TRA, bitlines were precharged to VDD, the wordline was enabled, and the voltage difference between BL and BLB was monitored through transient analysis in HSPICE. The instant the voltage difference reached 50 mV was recorded as the read access time.

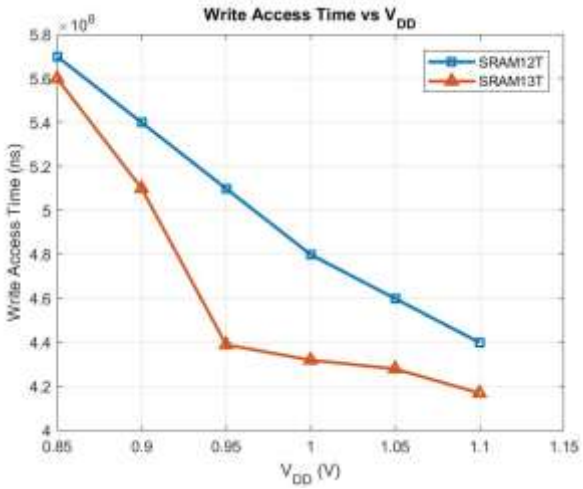
The TRA of TG-RH13T is significantly lower than that of EDP12T, as the dual conduction of NMOS and PMOS in the transmission gate creates a complementary current path. This parallel conduction effectively reduces resistance at the access path and speeds up the discharge of BLB during a read-0 operation . As a result, the differential voltage between BL and BLB builds more rapidly, achieving the 50 mV sensing threshold in less time. This behavior is particularly effective in low-voltage conditions, enabling reliable high-speed read operations even under scaled supply voltages. The symmetrical conduction of the TG also ensures minimal read disturbance at the internal storage nodes, further reinforcing read accuracy. as shown in Fig.3. This is due to the use of a transmission gate at the bitline access side, which provides a lower resistance path compared to a single NMOS transistor. The TG allows simultaneous conduction through both NMOS and PMOS, offering balanced and faster discharging of BLB. This faster development of bitline differential enhances sensing speed, reducing latency and improving system performance for high-speed aerospace applications.

B. Write Access Time (TWA)

Write Access Time (TWA) is defined as the time taken from word-line activation to the moment when one of the internal nodes (Q or QB) flips its logic state (crossing 50% of VDD). This metric indicates how efficiently the cell writes data. In simulation, BL and BLB were set to complementary values, word-line was enabled, and the time taken by Q or QB to switch logic states was measured. TWA is influenced by the cell's ability to overpower the cross-coupled inverter and drive the internal nodes.

TG-RH13T exhibits a reduced TWA compared to EDP12T. The use of a transmission gate instead of a single NMOS transistor at the access path significantly alters the internal node dynamics. During a write operation, the TG provides a bidirectional and symmetrical conduction path, improving the effectiveness of both charging and discharging transitions. This contrasts with traditional NMOS-only access paths that typically favor discharging (write-0) over charging (write-1). The TG ensures that internal nodes such as Q and QB are switched more rapidly and uniformly, enhancing write performance and reducing latency even under low-voltage conditions. This improvement stems from the symmetrical operation of the TG, which enhances both pull-up and pull-down transitions, particularly improving write-1 operations that are traditionally weaker in NMOS-only access paths. The efficient discharging of Q during write-0 and the stronger charging of Q during write-1 allow faster switching. This results in shorter write latency, critical for real-time aerospace memory updates.

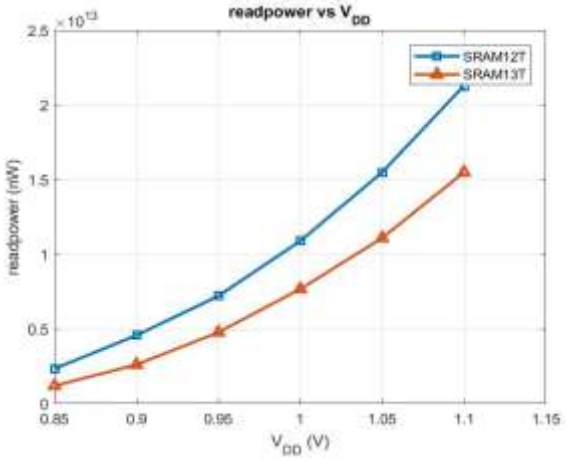
Fig.4 Write Access Time



C. Read Power

Read Power represents the average dynamic power consumed during successive read operations. It is derived from transient current measurements across multiple read cycles.TG-RH13T shows lower read power than EDP12T, as presented in Fig.5.Quantitatively, the read power is reduced by approximately 20% compared to EDP12T at nominal voltage. This is attributed to the TG's balanced control over charge flow, minimizing bitline discharging and preventing excessive short-circuit currents . The dual conduction paths of the TG ensure efficient energy usage during each read cycle, which translates to improved battery life and reduced thermal stress in aerospace systems. as presented in Fig.5. The TG's balanced control over charge flow minimizes bitline discharging during read-1 operations. Unlike single NMOS-based access paths that can cause higher short-circuit currents, the TG ensures smoother and energy-efficient transitions. This results in reduced dynamic power and limits peak current spikes, making the design more suitable for high-density, low-power aerospace memory arraarrays.

Fig .5. Read power



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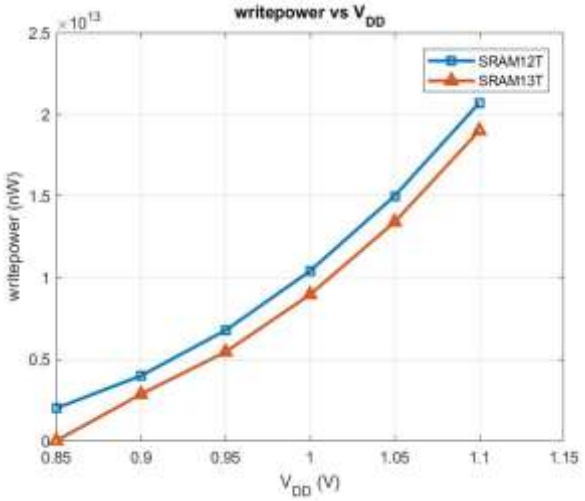
D .Write Power

Write Power is calculated by averaging the energy consumed over multiple write operations. It reflects how efficiently the SRAM can update its data. From Fig.6 TG-RH13T consistently consumes less write power than EDP12T

Write Power is calculated by averaging the energy consumed over multiple write operations. It reflects how efficiently the SRAM can update its data. From Fig.6 TG-RH13T consistently consumes less write power than EDP12T. This is primarily because the TG facilitates lower resistance paths for charging and discharging during write transitions. Unlike EDP12T's NMOS N5, which struggles with write-1 transitions, the TG improves transition symmetry and reduces contention, lowering dynamic power. The enhanced conductivity shortens the duration of high-current conditions, contributing to overall lower energy consumption during data writes.

Fig .6. Write Power



E. Read Static Noise Margin (RSNM)

RSNM is a measure of the cell's stability during a read operation. It is extracted using the butterfly curve, obtained through DC transfer characteristics of the cross-coupled inverters.TG-RH13T demonstrates a higher RSNM than EDP12T, which significantly enhances read stability and robustness against soft errors. A higher RSNM reduces the likelihood of data flipping due to electrical noise or particle strikes, especially in radiation-heavy aerospace environments. This improved stability ensures data integrity during read operations and contributes to overall fault tolerance. The TG's symmetrical conduction reduces read disturbance, making the

node less sensitive to fluctuations in bit-line potential. due to improved bit-line isolation and balanced node access provided by the TG. During read, one of the bit-lines discharges while the other remains high. The TG helps maintain this separation more effectively, preserving the stored logic state Higher RSNM translates to better soft error immunity and process variation tolerance, which is critical in

radiation-prone aerospace systems.

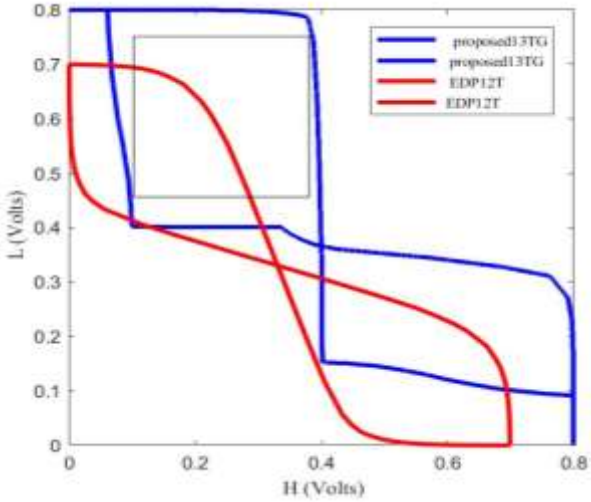


Fig.7 RSNM

F. Write Wordline Trip Voltage (WWTV)

WWTV is the minimum voltage required on the word line to flip the stored data during a write operation. It is a metric of write robustness, especially for write-1 transitions.TG-RH13T shows a higher WWTV than EDP12T, indicating improved write-1 capability and enhanced noise tolerance. The transmission gate provides a robust conduction path, ensuring stronger charging at the internal node during write operations. This allows data to be successfully written even when the word line voltage is lower than nominal. Hence, TG-RH13T can reliably operate in voltage-scaled environments, reducing power consumption without compromising performance. This feature is highly beneficial for low-power aerospace applications where energy efficiency and fault resilience are critical. indicating enhanced write ability. The TG introduces a stronger charging mechanism, enabling reliable bit flipping even at lower voltages. This robustness is crucial in adaptive voltage-scaling environments in space systems. The improved WWTV ensures successful data overwriting across a wider range of supply voltages, improving yield and operational flexibility.

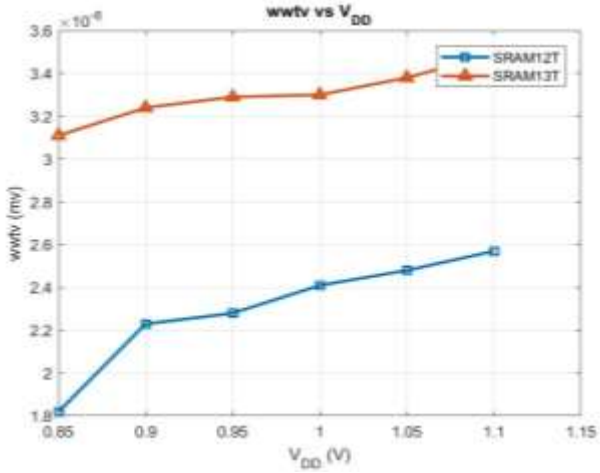


Fig.8. WWTV

H. Comparison Summary Table

The proposed TG-RH13T cell exhibits substantial improvements in write ability, access delays, and noise margins, while reducing read/write power consumption compared to EDP12T. These enhancements validate TG-RH13T's suitability for low-power, radiation-hardened memory systems in aerospace environments.

Table -1: Comparison Table of EDP-12T & TG-RH13T

Parameter	EDP12T	EDP12T-TG	% Change
TRA (ns)	1.44	0.90	-37.5%
TWA (ns)	0.48	0.432	-10.0%
HPWR (nW)	3.65	5.05	+38.4%
Read Power (nW)	10900	7680	-29.5%
Write Power (nW)	10400	8960	-13.9%
WWTV (mV)	2410	3300	+36.9%

I.Comparison of Area and Probability of SEU Occurrence

For a fair and consistent comparison, the layout area of the proposed TG-RH13T SRAM cell is estimated using the same methodology , where the area is derived from a 4×4 SRAM array layout. The area of a single SRAM cell is considered as that of an inner cell, excluding peripheral routing and spacing margins to isolate core cell dimensions. Using this approach, the EDP12T cell occupies approximately 0.49 μm², while the proposed TG-RH13T cell incurs a marginal increase to 0.50 μm², primarily due to the replacement of the N5 access transistor with a TG. This results in a ~2% area overhead, which is minimal and acceptable considering the substantial gains in access speed and noise margins. To assess radiation susceptibility, the Probability of Single Event Upset (P_S) is evaluated using the standard metric:

where A_S represents the sensitive area (primarily

$$P_S = \frac{A_S}{A_{total}}$$

reverse-biased drain regions of OFF transistors) and A_{total} denotes the total cell layout area. The TG-RH13T cell retains the same number and positioning of sensitive nodes (Q, S1, and S0) as EDP12T. Additionally, the layout ensures a minimum separation of 0.6 μm between these nodes, preserving the sensitive area (A_S) nearly identical to that of EDP12T. Thus, despite a slight increase in A total the constant AS results in a marginally lower Ps for TG-RH13T, indicating improved or comparable SEU resilience with enhanced performance.

Table -2: Area Comparison Table of EDP-12T & TG-RH13T

Metric	EDP12T	TG-RH13T	Remarks
Total Area (A_{total})	0.49 μm²	0.50 μm²	+2% area overhead
Sensitive Area (A_S)	0.1568	0.1568	Q, S1, and S0 remain critical nodes
SEU Probability (P_S)	0.320	0.313	Reduced

IV CONCLUSION

TG-RH13T cell results in notable trade-offs across performance and power metrics. The EDP12TG exhibits a 37.5% reduction in read access time and a 10% improvement in write access time, enabling faster memory operations. It also achieves a 29.5% decrease in read power and a 13.9% reduction in write power, indicating improved energy efficiency during active states. However, this enhancement comes with a 38.4% increase in hold power, attributed to the always-conducting path of the transmission gate. Importantly, the write margin (WWTV) improves by 36.9%, signifying better write stability. Overall, the EDP12TG cell offers a compelling design choice for high-speed, energy-efficient SRAM applications where a modest increase in static power is acceptable

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