IMPLEMENTATION OF MODIFIED HIGH-SPEED 32-BIT VEDIC MULTIPLIER IN FPGA

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ABSTRACT

The multiplier's speed is an important characteristic because it is a crucial component of many systems, including FIR filters, microprocessors, DSPs, etc. The multiplier determines how quickly the system operates because it is slower than the other components. An increase in the multiplier's speed will result in an increase in total speed. The speed of the multiplier is influenced by both the method of multiplication and the type of adder used for the addition of the partial products. The suggested Urdhva-Tiryakbhyam utilising Carry Save Adder (CSA) 32-bit Vedic multiplier architectures, which are based on Vedic sutra, have been realised. Nowadays, Vedic multipliers have emerged as one of many methods of multiplication. These sutras are designed to aid with quick calculations. In terms of speed, Urdhva-Tiryakbhyam is more effective than other multipliers. The evolved multiplier's ability to create all partial products in a single step is the Urdhva-Tiryakbhyam sutra's most important feature. The architecture substitutes high-speed adders for traditional Ripple carry adders to further reduce the latency. Lastly, the effectiveness in terms of speed is demonstrated by comparing the results with traditional multipliers. Using the Xilinx tool and Verilog, the effectiveness of the suggested method is synthesised and simulated.

Keywords: Vedic Multiplier, Urdhva-Tiryakbhyam sutra, Ripple Carry Adder, Carry Save Adder, FIR filter

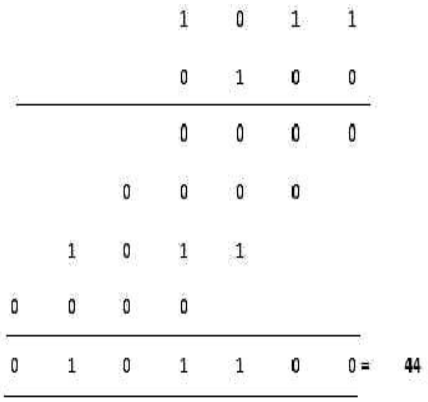
I INTRODUCTION

One of the crucial processes in signal processing and general-purpose processors is fast becoming high-speed multiplication. 16 Vedic sutras provide the foundation of Vedic mathematics. Mathematical processes are quick when performed utilising Vedic methods, and processing speed can be increased. Urdhva-Tiryakbhyam is the primary Vedic multiplication algorithm. When employing the Vedic Multiplier, two operands are multiplied both vertically and crosswise, and all the results are then added. By using the Vedic multiplier, the delay, area, and power will be efficient.

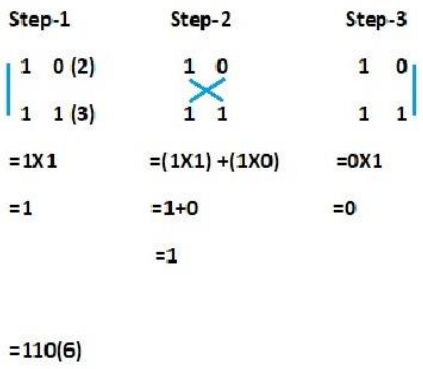
II URDHVA-TIRYAKBHYAM

One of the Vedic mathematical sutras, the Urdhva Tiryakbhyam Sutra, offers a fairly straightforward method for multiplying two decimal integers. Two binary values have been multiplied using the same method so that the procedure can be employed in digital systems. Urdhva Tiryakbhyam is the Sanskrit word which means vertical and crosswise respectively.

Normal multiplication



Vertical and Crosswise



III OBJECTIVE

- The objective of the implementation is to optimize the performance parameters such as area, delay, and power for the 32-bit Vedic Multiplier implementation using a carry-save adder.
- To design a 32-bit binary Vedic multiplier using Vedic sutras based on the Urdhva Tiryakbhyam method from ancient Vedic mathematics.
- To Design a high-speed Vedic multiplier with low power consumption for the application of FIR filter.

IV EXISTING METHOD

- Ripple carry adder is used for adding the multiplier output.
- It increases the critical path delay.

DISADVANTAGES:

- The area is increased and hardware complexity increases as the number of computations increases.
- Computational delay is high, and the performance of the design is low.

V PROPOSED METHOD

- The proposed method uses a carry-save adder.
- It is used to eliminate the critical path delay.
- It is simply a parallel ensemble of k full adders without any horizontal connection.

VI BLOCK DIAGRAM

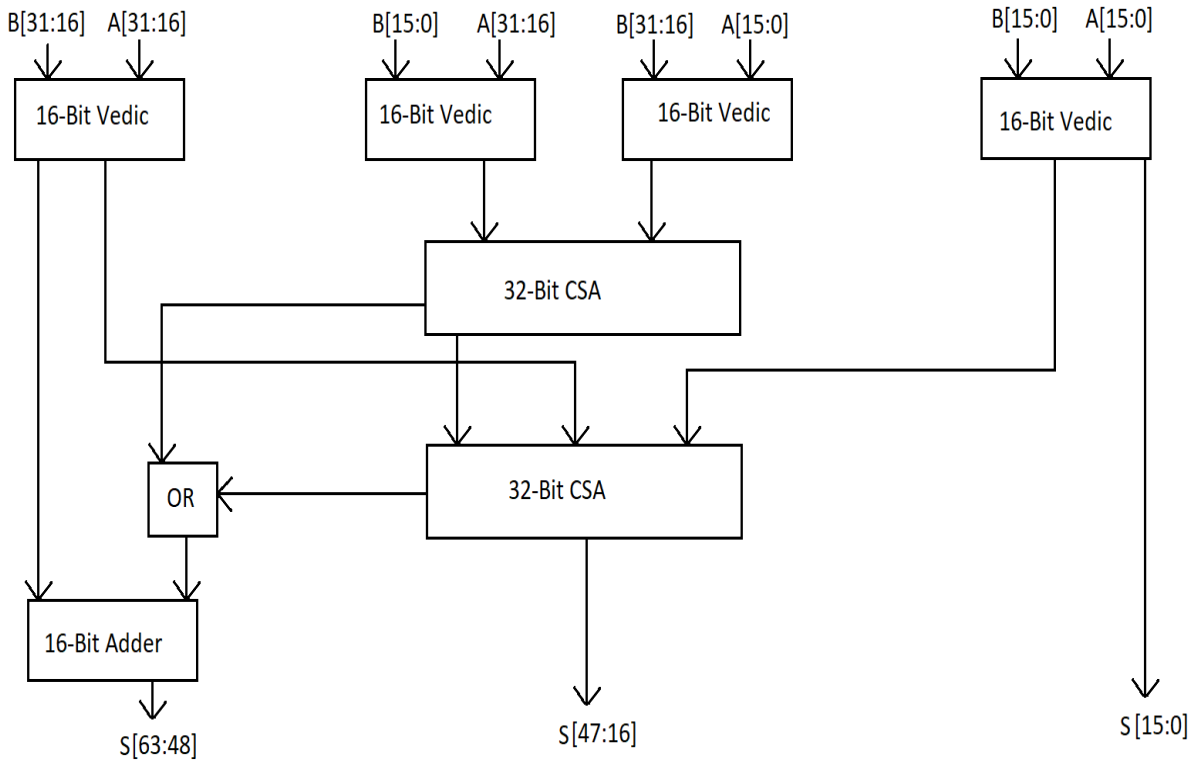


Fig 1 Block diagram

VII FIR FILTER

- A filter is a device or process that removes some unwanted noise or feature from a signal.
- FIR filter has finite duration because it settles to zero in finite time.
- These filters support high sampling rate for high-speed digital communication.

$$\boldsymbol{y(n) = \sum_{k=0}^{m-1} h(k)x(n-k)}$$

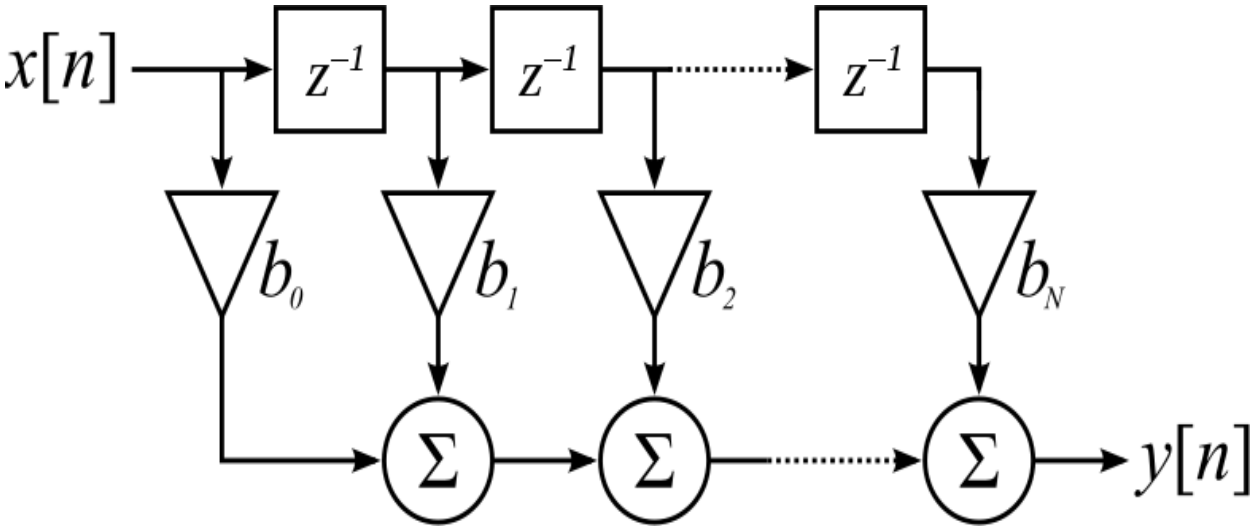
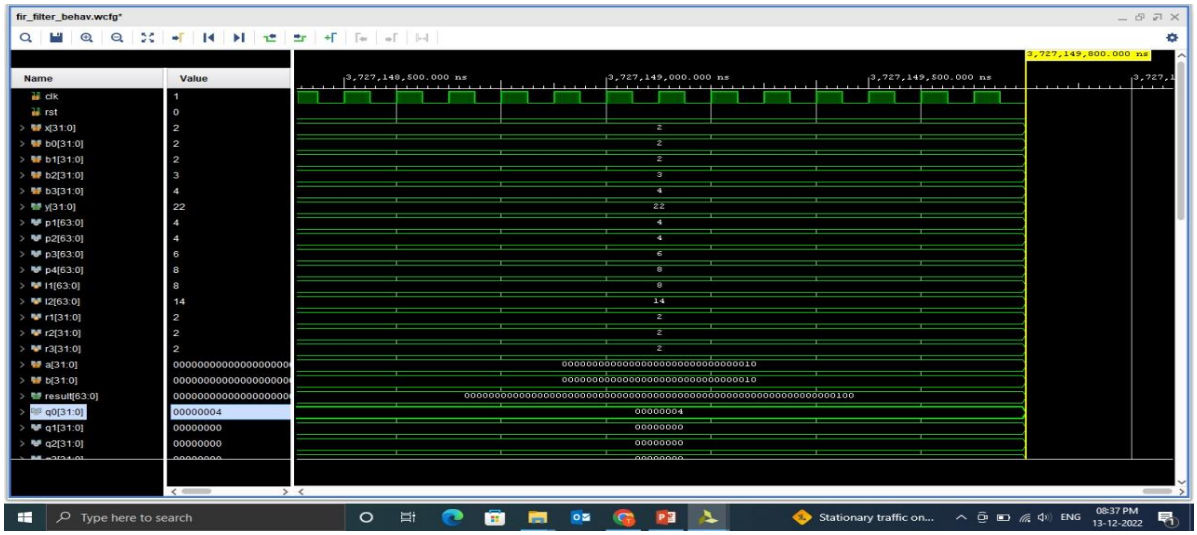


Fig 2 FIR filter

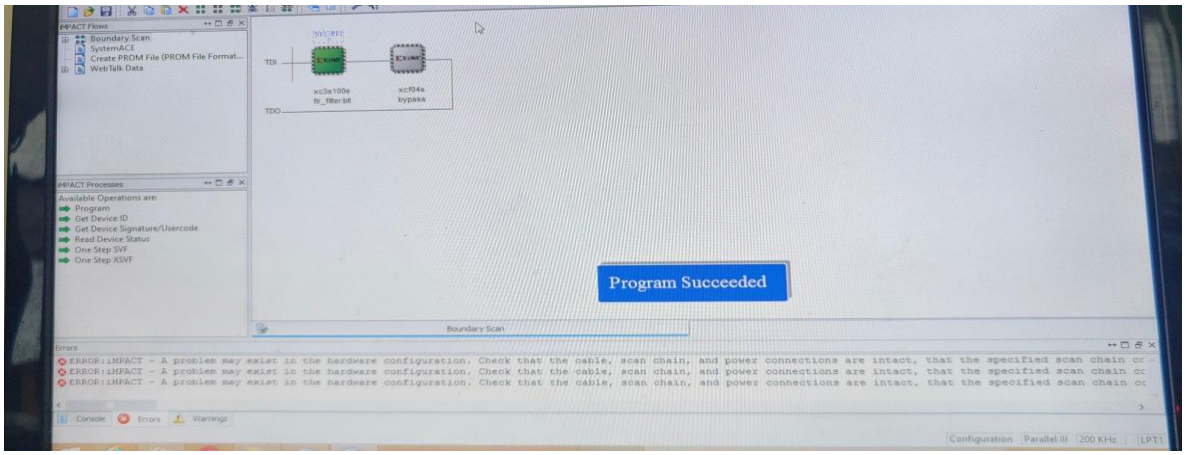
VIII METHODOLOGY

- A 4-bit Vedic multiplier is designed and in the same manner, the size of the Vedic multiplier is increased up to 32 bits i.e., 8-bit, 16-bit, and then 32-bit using RCA.
- And then by using CSA, the modified 4-bit Vedic multiplier is implemented and in the same way, the size of the modified Vedic multiplier is increased up to 32-bit i.e., 8, 16, and 32 bits.
- The final synthesis is done by using XILINX ISE 14.7 DESIGN SUITE

IX SIMULATION AND RESULTS



9.1 Simulation result of 32-BIT FIR FILTER Vedic multiplier



9.2 Program succeeded in hardware

9.3 Final output in FPGA

X COMPARISON OF EXISTING AND PROPOSED SYSTEM

S.NO	PARAMETER	EXISTING SYSTEM (using ripple carry adder)	PROPOSED SYSTEM (using carry save adder)
1	NO. OF 4-INPUT LUTs	3,065	2,810
2	DELAY	99.611ns	98.518ns
3	POWER	693mW	657mW

TABLE 1: COMPARISON OF EXISTING AND PROPOSED SYSTEM

XI APPLICATION

- Digital signal processing (DSP)
- Image processing

XII CONCLUSION AND FUTURE SCOPE

A 32-bit Vedic multiplier is constructed using VHDL and simulated on Xilinx ISE 13.2 utilising the Urdhva Tiryagbhyam Sutra of ancient Vedic mathematics. The performance factors such as several times, number of gates, and power are investigated, and it is discovered that the number of gates employed in the existing system is 18,390, while the suggested system has 16,899 and a time delay of 99.611ns out of 98.518ns. The proposed system consumes 657Mw of power. Four 16-bit multipliers, are used to construct one 32-bit multiplier, and a carry-save adder are used to create the multiplier. The hardware demand is high, which adds to the time delay. To achieve minimal time delay, the basic construction blocks should be minimised. The work is expandable to 64-bit. A symmetric architecture for a Vedic multiplier is also implemented. Improved lower-order multipliers and modified carry-save adders were then utilised to reduce the delay and the space occupied even further.

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