DESIGN OF 9-LEVEL YE PROGRESSION-BASED LADDER MULTI-LEVEL INVERTER

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***Abstract*—This paper proposes the design of a 9-level YE progression-based ladder multi-level inverter with a smaller number of power electronic components and lower switching losses. The proposed topology is designed in a ladder structure to reduce the design complexity. In this method, the carrier-free switching angle method is used to generate the digital pulse width modulation signals for the switches. Eight switching patterns are generated using Verilog and cross-compiled in the MATLAB Simulink Tool for verification. This topology generates multi-level inverter levels by utilizing positive or both wings of DC sources with switch controls and Voltage combinations of 1V and 3V are applied for DC sources. The effectiveness of the suggested approach is assessed for THD%, VPEAK, and VRMS.**

Keywords— Ladder Multi Level Inverter, Verilog, Switching Angle Method, Total Harmonic Distortion.

I. INTRODUCTION

Inverters are electronic devices that convert direct current (DC) to alternating current (AC), allowing DC energy sources to be used in AC-powered applications. Multi-level inverters are inverters that produce stepped voltage waveforms with numerous voltage levels, resulting in increased power quality, fewer harmonics, and improved voltage regulation. Multiple voltage levels are achieved by multi-level inverters by using numerous DC sources and varied switching configurations, which gives accurate manipulation of the output waveform. In high-power systems such as electric vehicles, renewable energy integration, and high-voltage motor drives, these inverters enable efficient and dependable AC power conversion. Multi-level inverters play an important role in furthering the integration of renewable energy sources (like photovoltaic) and improving the performance of power systems due to their capacity to enhance power delivery and improve energy efficiency [8]. Various approaches and topologies are used to reach higher voltage levels while using lower-power electronic components, depending on the circuits.

The need to lower component counts in multilevel inverter designs for cost-effectiveness, increased reliability, and decreased complexity [1] There are a few challenges, such as various switch needs, reduced redundancies, limited flexibility, unequal DC voltage distribution, and complex modulation schemes, that must be addressed in order to boost the usage of converters such as multi-level inverters in the power market [5]. In the switch-ladder inverters approach, the voltage from the preceding level is added with each increasing voltage level. The primary advantage of this design is that the failure of any switch does not result in the total output voltage becoming zero; instead, the voltage level across that single failed switch becomes zero. A minimum on-state voltage drop and power loss are present in the inverter [2]. The proposed method begins with the carrier-free switching angle method. The carrier-free switching angle approach involves applying mathematical formulas or algorithms to compute switching angles. To estimate the ideal switching timings of the switches, these equations take into account the required amplitude and phase of the output waveform. The carrier-free switching angle method provides additional freedom and control in structuring the output waveform by directly computing the switching angles. It allows for exact control of the harmonic content while lowering the total harmonic distortion (THD%) of the output waveform. Furthermore, the carrier-free switching angle approach has advantages in terms of lower switching losses and higher efficiency. Due to the absence of a carrier waveform, switching transitions are more optimized, resulting in lower power losses and improved overall system efficiency. There are four different strategies in the switching angle method. In comparison to other methods, the half-height switching angle method has a low THD of 8.37% [4]. The switch angle algorithm is digitally converted to 28 bits to generate switch patterns using Verilog. Switch patterns are validated by cross-compiling in MATLAB Simulink. With an increase in the number of levels, the THD can be reduced and a smooth sinusoidal waveform can be generated [3].

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II. PROPOSED METHOD

The proposed method is to obtain an AC waveform with low THD using a YE progression-based ladder inverter. This includes the generation of digital pulse width modulation using a carrier-free half-height switching angle algorithm to obtain switch patterns and a smooth waveform. Half-height SAM is used to generate the angles for different quadrants according to their levels. Later, the angles are converted into bits with a resolution of 2 to the power of 8 bits. The formula for generating the Half-Height Switching Angle Method is

$$\alpha_i = \sin^{-1}[(2i-1)/(m-1)]$$

where m is the level of the inverter.

i =1, 2, ….. (m-1)/2

The bits from 0 to 255 are taken practically and plotted with the obtained bits to get pulse width modulation for perfect results. YE Progression Laddered inverters consist of switches and DC voltages designed in a ladder structure to reduce the complexity of the circuit. The YE Progression is another novel or series progression, which derives from the fact that the value of the fourth term is equal to the sum of the previous terms (1st term, 2nd term, 3rd term) plus 1. The YE progression formula is taken as

$$\text{if } i \leq 3,\ V_i = i^2 - u(i-2)$$

$$\text{if } i \geq 4,\ V_i = 25 * 3^{i-4}$$

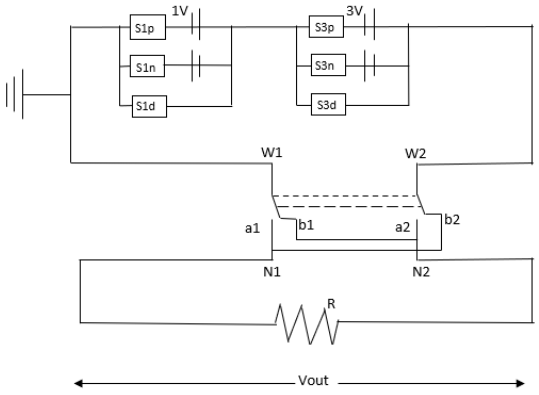
Where V_i is the input voltage.

The nine-level YE progression-based ladder inverter is constructed with two stages in both wings. The switches are connected to DC sources with voltages of 1 volt for the first stage and 3 volts for the second stage, with control switches for ON and OFF conditions. The circuit is connected as per the requirement with the mentioned components to operate the 9-level YE Progression Ladder Inverter. Voltage combinations are utilized in circuit design to regulate the ON and OFF states of switches as well as the rising and falling edges of levels, as shown in Table 1. The topology of the proposed 9-level YE progression-based inverter is shown in Fig. 1. The practically obtained results are performed in digital format to generate switching patterns that are controlled by digital pulse width modulation strategies with the suitable Verilog behavioral code. The suitable code uses an if-else condition for DPWM and switches (ON and OFF conditions). The rising and falling edges are formed by the switching patterns. In this ladder inverter, if one switch fails, the failed switch can be identified by performing the individual switch patterns for the various levels of voltage.

TABLE 1: VOLTAGE COMBINATIONS OF THE PROPOSED 9-LEVEL YE PROGRESSION -BASED INVERTER

Levels	***Positive Voltage Combinations***	***Levels***	***Negative Voltage Combinations***
0	0V	0	0V
1	1V	-1	-1V
2	3V-1V	-2	-3V+1V
3	3V	-3	-3V
4	3V+1V	-4	-3V-1V
3	3V	-3	-3V
2	3V-1V	-2	-3V+1V
1	1V	-1	-1V

Fig. 1. Topology for the Proposed 9-Level YE Progression-based Inverter



In this topology, V_{out} equals V_{N1N2}. If the switch is turned on, V_{w1w2}. If the switch is turned off, $-V_{w1w2}$. Switches ON and OFF condition depends on the switch patterns. This topology generates the rising and falling edges of the positive and negative half cycles of the voltage levels.

III. RESULTS AND DISCUSSION

The proposed 9-level YE progression-based ladder inverter is developed to generate an AC waveform with low harmonics by using DPWM signals and switching patterns. The DPWM signals are derived from the Half Height Switching Angle Method and generated using Verilog behavioral code in Xilinx. By applying logic gates to the DPWM signals, switches are formed to generate the switching patterns. Fig. 2 shows the generation of switch patterns for the 9-level YE progression-based ladder inverter.

Fig. 2: Switch patterns for the proposed 9-level YE progression-based ladder inverter in Xilinx Software.

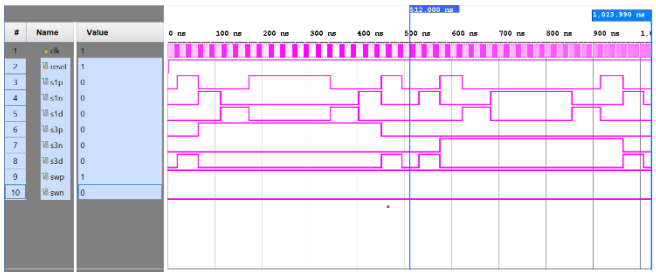
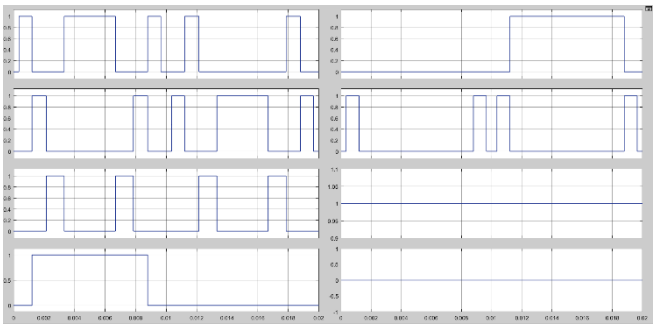


Fig. 3. Switch patterns of the proposed 9-level YE progression-based inverter using Matlab Simulink.



In the scope window, switch patterns are formed. At 50Hz, the time required to run the positive and negative cycle of the waveform is 0.02. There are both positive and negative voltage combinations in the switch pattern.

Fig. 4: Simulink Model for the Proposed 9-Level YE Progression-Based Inverter.

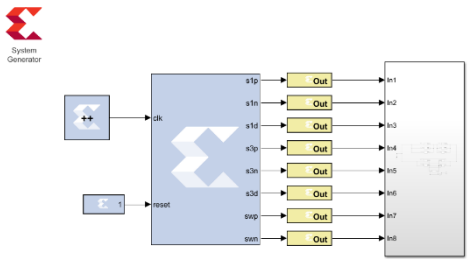


Fig. 5. Generated AC output for the proposed 9-level YE progression-based inverter.

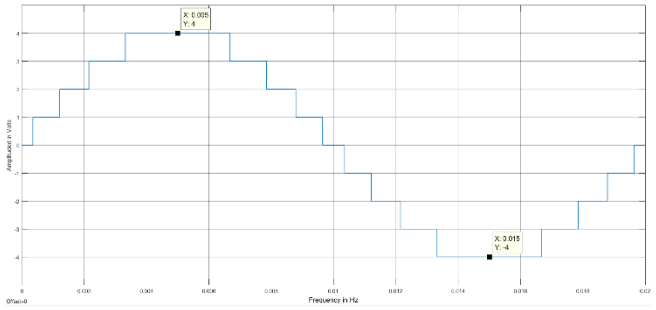


Fig. 6. a. %THD of the proposed 9-level YE progression-based inverter

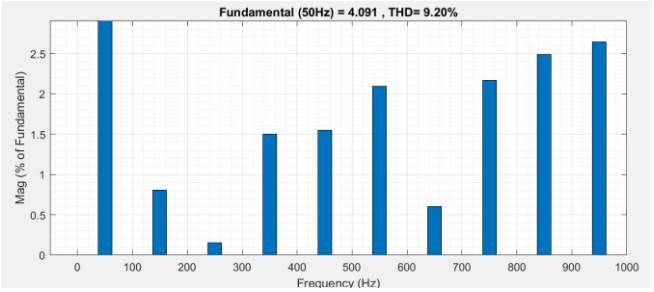
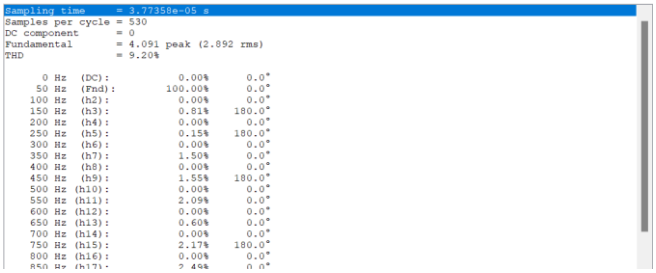


Fig. 6. b. Fundamental values of the proposed 9-level YE progression-based inverter.



```
Sampling time      = 3.77358e-05 s
Samples per cycle  = 530
DC component       = 0
Fundamental        = 4.091 peak (2.892 rms)
THD                = 9.20%

    0 Hz  (DC):          0.00%      0.0°
   50 Hz  (Fnd):       100.00%      0.0°
  100 Hz  (h2):          0.00%      0.0°
  150 Hz  (h3):          0.81%    180.0°
  200 Hz  (h4):          0.00%      0.0°
  250 Hz  (h5):          0.15%    180.0°
  300 Hz  (h6):          0.00%      0.0°
  350 Hz  (h7):          1.50%      0.0°
  400 Hz  (h8):          0.00%      0.0°
  450 Hz  (h9):          1.55%    180.0°
  500 Hz (h10):          0.00%      0.0°
  550 Hz (h11):          2.09%      0.0°
  600 Hz (h12):          0.00%      0.0°
  650 Hz (h13):          0.60%      0.0°
  700 Hz (h14):          0.00%      0.0°
  750 Hz (h15):          2.17%    180.0°
  800 Hz (h16):          0.00%      0.0°
  850 Hz (h17):          2.49%      0.0°
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The topology of the circuit is designed in the subsystem and the black box's switching patterns are linked to the subsystem's input, as shown in Fig. 4. The topology is designed with the DC voltages of 1V and 3V controlled by the switches. and the scope is connected to the circuit design to generate AC output, as depicted in Fig. 5. %THD and fundamental values can be formed with the generated waveform for the proposed 9-level YE progression-based inverter, as shown in Fig. 6.

IV. Conclusion

The proposed 9-level YE progression-based ladder inverter has been simulated and cross-compiled in Matlab Simulink. The proposed topology is advantageous in terms of the number of components used. The effectiveness of the suggested approach is evaluated based on key performance metrics, including total harmonic distortion (THD%), VPEAK, and VRMS. The results obtained demonstrate the superior performance of the proposed design in terms of achieving 9.20% lower THD for 9 levels and voltage peaks of 4.091V. As the number of levels increases, a low THD with a smoother sinusoidal waveform can be obtained. As part of future work, the proposed method can be implemented. It is possible to develop the proposed Ye progression-based inverter for more advanced levels.

Acknowledgment

A successful project is never completed with a single effort or by the person who is assigned to it; rather, it always requires the guidance and supervision of an expert who either actively or passively assists the undersigned in completing the job.

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