ADAPTIVE DIGITAL PREDISTORTION FOR SDR USING FPGA

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***Abstract*—A method for minimising distortion in communication networks is adaptive digital predistortion (DPD). A technique known as Software Defined Radio (SDR) makes it possible to modify radio equipment using software, giving communication networks more flexibility. Integrated circuits that may be programmed to carry out certain tasks are called field programmable gate arrays (FPGAs). According to the abstract you gave, an FPGA-based adaptation of DPD for SDR is being developed. In comparison to conventional hardware-based DPD techniques, this implementation is likely to have more flexibility, reconfigurability, and scalability. The software used to programme the FPGA to carry out the required signal processing operations is most likely a component of the FPGA-based adaptive DPD for SDR implementation. This method gives the communication system more flexibility in responding to changes, allowing it to adju shifting needs and circumstances.**

***Index Terms*—DPD, SDR(Software Defined Ra FPGA(Field Programmable Gate Array), Nonlinear Distor Linearization**

I. INTRODUCTION

Wireless communication tools have become indispensable part of everyone's everyday lives as techno advances. High-speed connections are necessary for the ph video, data, and other applications on these communica devices. The fifth generation (5G), which uses a distinct s networking protocols, has supplanted the second genera (2G) of commercial wireless communication technolo Since every time a new generation of wireless communica standard is established, all communication devices mus updated. It takes significant planning and money to a communication equipment for numerous communica protocols. A quick-to-adapt, programmable communica system that is flexible, reconfigurable, and hardware-free thus seen a significant rise in demand.

SDR, sometimes referred to as software-defined radio, effective remedy for these issues. In the telecommunications sector, SDR is a fast evolving technology that aims to provide a flexible and adaptable transceiver architecture. Without changing the hardware on which they are implemented, SDRs' capacity may be raised. Because of this characteristic, SDR may create a flexible transceiver that conforms with any kind of communication standard. These SDR-based programmable communication devices may be capable of supporting both current and future wireless communication standards and network protocols. Baseband signal processing techniques and communication network protocols are implemented in SDRs on a reprogrammable hardware platform, allowing for updates without altering the hardware. Consequently, the issue of whenever a network is upgraded from one generation to the next, the burden of device upgrades will decrease. Due to these benefits, SDR-based transceivers have largely replaced analogue transceivers in recent years for a variety of wireless communication applications.

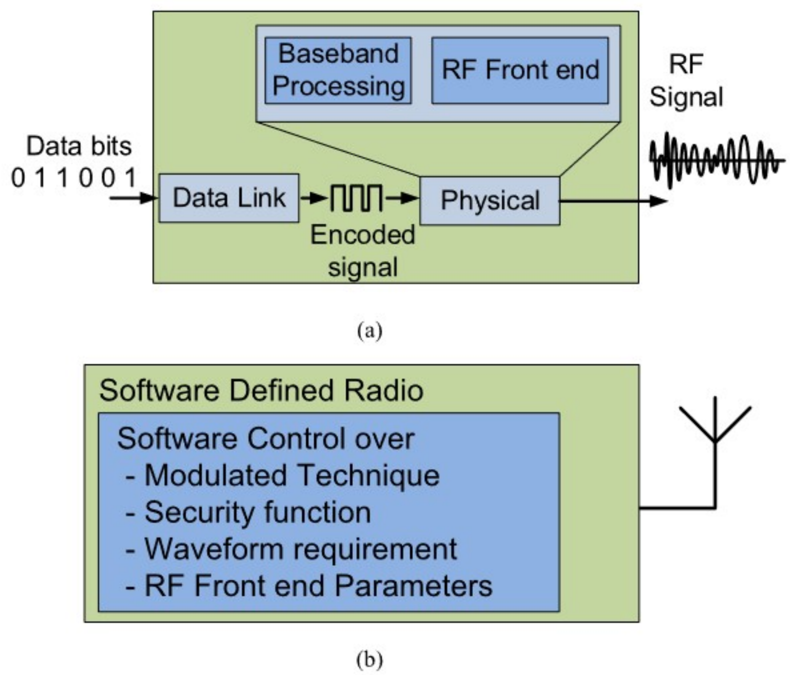

Fig. 1. (a) SDR role in OSI layers, (b) SDR properties.

SDR-based transceivers typically function at the data connection layer and physical layer, the bottom two levels of the OSI architecture, as seen in Fig. 1. Using a flexible and adaptable hardware architecture, SDR transceivers implement some or all of the software-defined transceiver features. Systems with field-programmable gate arrays (FPGA), general-purpose processors (GPP), embedded processors, and programmable system-on-chip (SoC) are examples of adaptive and reconfigurable systems. By incorporating new features and capabilities, these platforms enable upgrading an existing transceiver system without the need to buy new hardware. The physical layer of SDR transceivers is made up of two sub-blocks, the baseband processing block and the radio frequency (RF) front end block, as seen in Fig. 1 (a). As The baseband processing block performs the task for which it is named. handles, Baseband signal generation, modulation, demodulation, encoding, and decoding, as well as link-layer protocol implementation, are just a few examples. DSP processors, embedded processors, and FPGAs are required for baseband processing. On the other hand, RF transceiver circuitry is utilised at the RF front end to send and receive signals at various RF carrier frequencies as well as to convert baseband to RF and RF to baseband signals. A universal hardware/software co-platform with DSP processors/embedded processors, FPGAs, and programmable RF front end makes up SDR-based transceivers. Using these SDR transceivers, software can control the majority of transceiver characteristics, including waveform specification requirements, information security functions, signal modulation/demodulation techniques, RF front end settings, etc. Fig. 1 (b) illustrates this.

II. ADP for SDR using FPGA:

Real-time signal processing, which is best done in hardware, is necessary for the ADP technique. The speed and adaptability of FPGAs make them ideal for real-time ADP algorithm execution. The pre-distortion filter and the non-linear model of the power amplifier are the two fundamental elements of the ADP approach.

The look-up table (LUT), which transforms the input signal into the output signal, frequently implements the non-linear power amplifier concept. The output of the power amplifier is assessed for a variety of input signals in order to produce the LUT. The gathered data is then fitted to a model.

A method for reducing distortion in radio frequency (RF) power amplifiers (PA) used in wireless communication systems is adaptive digital predistortion (ADP). The broadcast signal could be corrupted as a result of RF PAs' typical nonlinear nature. By calculating the nonlinear behaviour of the PA and pre-distorting the transmitted signal to account for it, ADP can assist in correction for this distortion.

A radio communication system that uses digital signal processing to create hardware-typically implemented components in software is known as a "software-defined radio" (SDR). Communication system design and deployment are thus more flexible and adaptive.

In order to create digital circuits, FPGAs (Field-Programmable Gate Arrays) are a form of hardware that is frequently utilised in SDR systems. Due to their excellent performance and adaptability, FPGAs can be used to implement ADP algorithms in SDR systems.

The benefits of lowering power consumption in terms of cost-saving are now being investigated in continuing research on the standards for wireless communication equipment. Additionally, communication standards include linearity requirements, necessitating the reduction of unacceptable distortions. Emerging standards that enhance high data rates utilising spectrally efficient sophisticated modulation methods need for power amplifiers (PAs) that can handle signals with high peak-to-average power ratios (PAPRs).

Unfortunately, because of the PA nonlinear behaviour, those spectrally efficient modulation formats are extremely susceptible to the intermodulation distortion (IMD) that results from nonlinearities in the RF transmitter chain. This suggests that large backoff (BO) levels are necessary for linear amplification, which would reduce the PA's power efficiency. For example, in the case of cellular telephony, PAs must support members of the CDMA family of wireless technologies, including CDMA2000, Evolution Data Optimised (EVDO), WCDMA, and Long-Term Evolution (LTE), which have average PAPR values of around 10 dB. In a broadband access environment, communication protocols like IEEE 802.11a, DVB-T, or the IEEE 802.16, which permit even higher PAPRs (up to 14 dB), employ orthogonal frequency division multiplexing (OFDM) signals.a bandwidth of at least 20 MHz. The PA in base stations must also manage a composite RF signal that is produced by mixing various individually modulated carriers. The linearity vs. efficiency issue is made worse by the wider bandwidths and greater PAPR levels. The employment of PA linearizers is one well-known technique for halting the power-inefficient BO process.

III. Methodology

An approach used to account for the nonlinear distortion in radio frequency (RF) power amplifiers is adaptive digital predistortion (ADP). ADP aims to increase the linearity and efficiency of RF power amplifiers. ADP may be implemented in Software-Defined Radio (SDR) utilising Field Programmable Gate Arrays (FPGAs).

A. State-Of-The-Art

The literature describes a number of DPD models, but the bulk of them use commercially accessible equipment for transmission and reception and a fixed sample set of the input baseband signal. Predistorted signals are produced on a personal computer (PC) running MATLAB, and the required system/PA modelling is carried out offline. This predistorted signal is instantly sent into the signal generators to gauge the system's efficacy. These DPD systems cannot be viewed as real-time solutions because they require pricey commercial equipment and perform all processing offline. Such DPD solutions do not have the real-time adaptability to change the DPD parameters automatically because the DPD coefficient extraction is carried out externally.

To assess the DPD performance, a co-simulation test setup is developed, where the DPD coefficients are retrieved in MATLAB and uploaded to the LUTs of the FPGA design. In the literature, memory polynomial and memoryless polynomial-based DPD solutions are put forth. These solutions are then tested in hardware using a predetermined sample set of the input signal on a board before being sent into the computer for further processing. The predistorted signal is created by determining the DPD coefficients. This signal is then sent back to the FPGA board for RF transmission. Due to the fact that DPD is carried out on a PC, such solutions cannot be referred to as real-time systems. A set of DPD is used in a suggested adaptive DPD system to handle the dynamic features of PA. Using the MATLAB deep-learning toolbox, the initial DPD coefficients for the proposed adaptive system are offline computed for various PA output powers and temperatures. A particular set of DPD coefficients are produced and stored by an FPGA's LUTs. In these systems, PA acts as the DPD coefficient. If the PA unit is changed, manual help will be needed. The fact that manual intervention is required for the adaption means that these DPD systems cannot be employed as a real-time adaptive DPD solution.

Various commercial SDR systems are mentioned in the literature as well. However, the majority of these systems only offer a modest amount of reconfigurability for the production of the necessary signals with the required bandwidth and sampling frequency [29]–[31]. Furthermore, the addition of user-specific applications is not supported by these platforms. The universal software radio peripheral (USRP) SDR transceivers from National Instruments (NI) [32] address the aforementioned problem. The absence of an application programming interface (API) through LabVIEW (NI software) is another issue with NI USRP. As a result, all programming, user-specific application implementation, and upgrades must be done on a separate PC running LabVIEW.

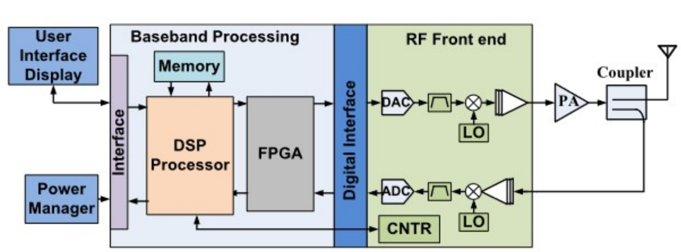

Fig. 2. SDR based transmitter architecture.

As illustrated in Fig. 2, a LUT-based real-time adaptive DPD (ADPD) solution is created and put into practise on a programmable and adaptable SoC platform. The suggested architecture offers a hardware-software interface for building an SDR-based transceiver system that is capable of producing and transmitting a variety of baseband signals in real time to a number of RF carrier frequencies. Through Real-time DPD, the suggested SDR transceiver could simultaneously reduce the PA nonlinearities. The temperature and the characteristics of the input signal affect how PA behaves. In order to adapt to these changes without requiring human input, DPD must be adaptable. The real-time flexibility of the suggested approach, which enables the DPD coefficient to be immediately recalculated, satisfies this need.

The three main steps in the building of the SDR transceiver using the real-time ADPD method are baseband signal generation, characterising PA nonlinear characteristics, and applying the inverse nonlinear characteristics of PA in LUTs to linearize the system. The PA in the saturation region drives a genuine LTE signal. Using the input and output of PA, the amplitude and phase distortion contributed by the transceiver system and PA are calculated. Following the computation of this data, the system's inverse gain and phase as well as the nonlinear properties of the PA are generated and saved in the LUTs. LUTs are used in the FPGA to synthesise the predistortion function, which is the outcome of the PA characterization. The proposed immediate Real-time nonlinearities in the system/PA are removed by the The predistorter coefficients may be updated while data is being sent using the ADPD approach. When system performance drops below the required level, predistorter coefficients are only updated in real-time. Based on anticipated system performance, the real-time ADPD can be automatically engaged and disabled to reduce power consumption and extra calculations.

IV. PROPOSED METHOD

The recommended approach of adaptive digital predistortion for software-defined radio (SDR) is implemented on field-programmable gate arrays (FPGAs) in order to improve the linearity and performance of SDRs. Since the DPD method is adaptable, it can change its parameters in response to changes in the input signal, which enhances performance and reduces errors. FPGAs are used because they offer speedy processing, low latency, and low power consumption. The recommended approach consists of the subsequent actions:

1) An analog-to-digital converter, or DC, digitises and samples the input signal.
2) The FPGA receives the digitised signal and uses it to launch the DPD algorithm.
3) The output of the FPGA is a pre-distorted signal. Reduced distortion and enhanced linearity are the outcomes of the transmitter's non-linearities being offset by the predistorted signal.
4) As the input signal changes, the DPD algorithm is adaptable and constantly alters its settings.

Software-Defined Radio (SDR), a type of radio communication system, substitutes the hardware components with software to provide flexibility, reconfigurability, and application-specificity. SDRs commonly have non-linearities, which can enhance distortion, restrict range, and impair performance. Non-linearities in the transmitter can be caused by a variety of factors, such as signal clipping, memory effects, and amplifier saturation. These issues are typically addressed by SDRs by using Digital Predistortion (DPD) to account for the non-linearities of the transmitter. By creating a model of the non-linear behaviour of the transmitter, DPD predistorts the input signal before it is broadcast. The aim of DPD is to cancel out.

However, DPD requires real-time processing of the input signal and is a computationally demanding task. FPGAs (Field Programmable Gate Arrays) are useful in this situation. FPGAs are digital logic devices with the ability to be programmed to carry out challenging DPD tasks. FPGAs are the perfect platform for implementing DPD in SDRs since they have fast processing rates, little latency, and little power consumption. An adaptive DPD algorithm that has been built on an FPGA is used in the suggested approach of adaptive digital predistortion for SDR. The algorithm improves efficiency and lowers mistakes by continually updating its settings in response to changes in the input signal. The technique is more efficient than conventional fixed DPD algorithms because of its adaptive nature. can only fix a particular set of non-linearities. improved linearity and less distortion are the result of the transmitter's nonlinearities. The recommended approach of Adaptive Digital Predistortion for SDR Employing FPGA is a way for improving the linearity and performance of SDRs by utilising an adaptive DPD algorithm built on FPGAs. The use of FPGAs makes it feasible to process input signals in real-time, and the algorithm's adaptive nature enhances performance and reduces distortion.

A. *Hardware Implementation and Measurement*

The ADRV9371 evaluation board from the analogue device is utilised as an RF front end, while the Xilinx zynq SoC ZC706 evaluation board serves as a SoC. Figure depicts the experimental setup employed in this study. ADRV9371 maintains synchronisation between the transmitter and receiver by using a single chip for both signal transmission and reception. Fixed point algorithms, which are more complicated than integer-based algorithms, are needed for PDU implementation in FPGA. The DAC and ADC on the RF transceiver board each have a size of 16 bits and 14 bits, respectively. As a result, the produced baseband signal is stored in the transmission route with a 16-bit resolution, whereas the received data is stored with a 14-bit resolution. The LUT that was used To cover every potential magnitude of the baseband modulated signal, 4096 values were used. In terms of NMSE, power spectral density (PSD), error vector magnitude (EVM), and hardware utilisation, the performance of the suggested technique is compared. Following the decoding of the symbols in the received signal, the EVM is calculated. It shows the discrepancy between the original symbol location and the detected symbol position. The gain and phase values of the signal are multiplied by the address of the BRAMs to produce the predistorted signal. The architecture for creating the predistorted signal using the LUT-based memory polynomial ADPD is shown in Fig. 8. The preconditioning of the baseband signal to make the system linear is shown by the three sets of PDU that were shown in Fig. 8. Each According to the value of m, PDU's LUTs store the inverse gain and phase values. PDU inputs are consequently compounded with different gain/phase settings. The PDU receives the baseband signal for m = 0 and records the inverse gain/phase for m = 0. When m = 1, the input signal is In the PDU calculated for m = 1 and m = 2, the input signal is multiplied by inverse gain/phase and delayed by 1 sample for m = 1 and by 2 samples for m = 2, respectively. The PDU outputs are combined to generate the predistorted signal, which is then delivered to the RF transceiver board for transmission.

B. *Software defined radio*

A software radio (SR) is a transmitting/receiving device where all essential processing is done by software in high speed signal processing components, with digitising happening at (or very close to) the antenna. Although there are many other definitions in the literature (such as "more user-friendly radio," "radio with personalization and software download on demand," etc.), from the perspective of hardware design, this one is probably the most accurate.

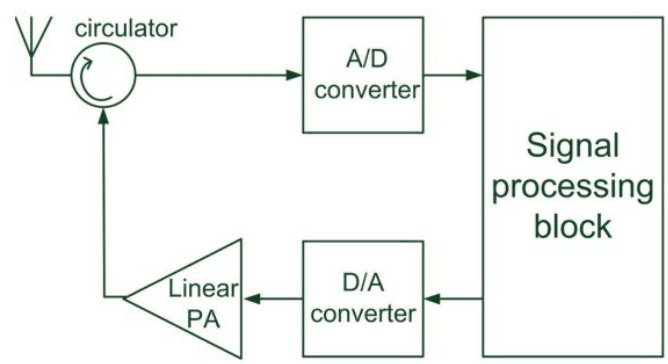

Fig. 3. Basic concept of a software radio.

A simple antenna, a signal processing block, data converters, a power amplifier, a circulator, and a power amplifier are all that the perfect software radio would need. A number of problems exist with this idea, such as the requirement for high-speed data converters, the requirements for real-time signal processing, or the capability to evaluate weak signals. The bulk of genuine current transceivers employ a concept known as Software Defined Radio (SDR), which is thus more or less the ultimate aim. According to the definition of an SDR [14], a radio is one that performs receive digitization downstream from the antenna, typically after wideband filtering, low noise amplification, and down conversion to a lower frequency in later stages with a reverse method of transmit digitization, is taking place. Digital signal processing defines the radio's characteristics in adaptable and re-configurable functional components.

Several software defined radios are currently available on the market. The Blade RF, developed and produced by NUAND Company, and the Universal Software Radio Peripheral (USRP), from Ettus Research (now National Instruments), are two families of devices that are possibly the most well-known in the research world. With the exception of USRP1, all devices in the USRP family enable MIMO and may be used with a range of frontends, such as LFTX/RX (covering the DC to 30 MHz frequency range), WBX (covering the 50-2200 MHz frequency range), TVRX2 (covering the 50-860 MHz frequency range), or the most recent CBX-120 (1200-6000 MHz). The BladeRF radios span the 300-3800 MHz frequency spectrum (with extension to 60kHz-300 MHz), feature a fixed front-end based on an LMS6002 microprocessor, and are MIMO scalable to 2x2 (x40) or 4x4 (x115).

Device type	FPGA	Bus	Bandwidth	A/D converters
USRP	Altera	USB 2.0	8 MHz	12bit, 64 MSa/s.
USRP2	Spartan 3A	Gig.ETH	25 MHz	14bit, 100 MSa/s.
USRP N210	Spartan 3A	Gig.ETH	25MHz	14bit, 100 MSa/s.
USRP E110	Spartan 3A+OMAP3	Gig.ETH	8MHz	12bit, 64 MSa/s.
USRP X310	Kintex 7	1/10Gig.ETH	120MHz	14bit, 200 MSa/s.
BladeRF x40	Cyclone 4E	USB 3.0	28 MHz	12 bit, 40 MSa/s.
BladeRF x115	Cyclone 4E+ARM9	USB 3.0	28 MHz	12 bit, 40 MSa/s.

Fig. 4. Parameters of selected SDR devices.

Before you begin to format your paper, first write and save the content as a separate text file. Complete all content and organizational editing before formatting. Please note sections IV-C–IV-G below for more information on proofreading, spelling and grammar.

Keep your text and graphic files separate until after the text has been formatted and styled. Do not number text heads—LaTeX will do that for you.

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Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Abbreviations such as IEEE, SI, MKS, CGS, ac, dc, and rms do not have to be defined. Do not use abbreviations in the title or heads unless they are unavoidable.

D. Units

- Use either SI (MKS) or CGS as primary units. (SI units are encouraged.) English units may be used as secondary units (in parentheses). An exception would be the use of English units as identifiers in trade, such as "3.5-inch disk drive".
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- Use a zero before decimal points: "0.25", not ".25". Use "cm^3", not "cc".)

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Number equations consecutively. To make your equations more compact, you may use the solidus (/), the exp function, or appropriate exponents. Italicize Roman symbols for quantities and variables, but not Greek symbols. Use a long dash rather than a hyphen for a minus sign. Punctuate equations with commas or periods when they are part of a sentence, as in:

$$a + b = \gamma \tag{1}$$

Be sure that the symbols in your equation have been defined before or immediately following the equation. Use "(1)", not "Eq. (1)" or "equation (1)", except at the beginning of a sentence: "Equation (1) is . . ."

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Please use "soft" (e.g., `\eqref{Eq}`) cross references instead of "hard" references (e.g., `(1)`). That will make it possible to combine sections, add equations, or change the order of figures or citations without having to go through the file line by line.

Please don't use the `{eqnarray}` equation environment. Use `{align}` or `{IEEEeqnarray}` instead. The `{eqnarray}` environment leaves unsightly spaces around relation symbols.

Please note that the `{subequations}` environment in LaTeX will increment the main equation counter even when there are no equation numbers displayed. If you forget that, you might write an article in which the equation numbers skip from (17) to (20), causing the copy editors to wonder if you've discovered a new method of counting.

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LaTeX can't read your mind. If you assign the same label to a subsubsection and a table, you might find that Table I has been cross referenced as Table IV-B3.

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G. Some Common Mistakes

- The word "data" is plural, not singular.
- The subscript for the permeability of vacuum μ_0, and other common scientific constants, is zero with subscript formatting, not a lowercase letter "o".
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- In your paper title, if the words "that uses" can accurately replace the word "using", capitalize the "u"; if not, keep using lower-cased.
- Be aware of the different meanings of the homophones "affect" and "effect", "complement" and "compliment", "discreet" and "discrete", "principal" and "principle".
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Text heads organize the topics on a relational, hierarchical basis. For example, the paper title is the primary text head because all subsequent material relates and elaborates on this one topic. If there are two or more sub-topics, the next level head (uppercase Roman numerals) should be used and, conversely, if there are not at least two sub-topics, then no subheads should be introduced.

J. Figures and Tables

a) Positioning Figures and Tables: Place figures and tables at the top and bottom of columns. Avoid placing them in the middle of columns. Large figures and tables may span across both columns. Figure captions should be below the figures; table heads should appear above the tables. Insert figures and tables after they are cited in the text. Use the abbreviation "Fig. 5", even at the beginning of a sentence.

TABLE I
TABLE TYPE STYLES

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Fig. 5. Example of a figure caption.

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CONCLUSION

The created SDR transceivers provide a practical, flexible, and cost-effective solution to build multifunctional transceivers that are easy to adjust via software control. DPD design for SDR transceivers is being used to provide advanced LTE transmissions. A quick SoC shortens the time required extracting coefficients. A memory polynomial is used when nonlinearity of order 9 and memory depth of order 2 are coupled. The performance of the proposed technique is evaluated using NMSE, EVM, and ACPR calculations. The system performance is unaffected by the PDU's performance, according to calculations. When tested with a 20 MHz LTE signal sent over a 10W PA, the suggested approach shows a noticeable improvement after linearization.

Adaptive digital predistortion (DPD) is a technique used in software-defined radio (SDR) to lessen the effects of nonlinear distortion in power amplifiers (PAs). DPD is a feasible alternative for SDR applications since it can be implemented in an FPGA to achieve real-time processing with little delay. In conclusion, using an FPGA for adaptive DPD in SDR has several advantages, including speedy processing speeds, low latency, and the ability to handle enormous data quantities. This technique can improve the overall performance of SDR systems and increase their usefulness in real-world applications. FPGA-based DPD does have certain disadvantages, though, namely the possibility for increased power consumption and the need for highly developed hardware design abilities. However, the Future SDR systems have a chance to Adaptive digital predistortion (DPD) is a technique used in software-defined radio (SDR) to lessen the effects of nonlinear distortion in power amplifiers (PAs). DPD is a feasible alternative for SDR applications since it can be implemented in an FPGA to achieve real-time processing with little delay. In conclusion, using an FPGA for adaptive DPD in SDR has several advantages, including speedy processing speeds, low latency, and the ability to handle enormous data quantities. This technique can improve the overall performance of SDR systems and increase their usefulness in real-world applications. FPGA-based DPD does have certain disadvantages, though, namely the possibility for increased power consumption and the need for highly developed hardware design abilities. However, the Future SDR systems have a chance to gain from the advantages of FPGA-based DPD.

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